FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-22110-4E

ASSP Communication Control

155-Mbps ATM Transceiver

MB582A/583A

■ DESCRIPTION

The MB582A and MB583A are the chip set that forms a transceiver used for high-speed, point-to-point communications over optical fibers such as in ATM-LAN (asynchronous transfer mode LAN), SDH (synchronous digital hierarchy), and SONET (synchronous optical network).

The MB582A transmitter chip generates a high-frequency clock signal from a low-frequency reference clock signal using an internal phase-locked loop (PLL). With the generated clock, the MB582A multiplexes eight-channel parallel data into single-channel serial data.

The MB583A receiver chip extracts and regenerates the regenerated clock signal from received serial data using an internal PLL. With the regenerated clock, the MB583A demultiplexes single-channel serial data into eight-channel parallel data.

■ FEATURES

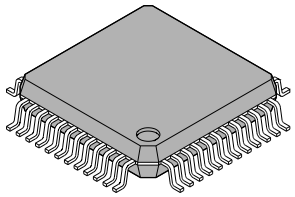
- Applicable to ATM, SDH, and SONET
- 155.52-Mbps serial data transmission
- Internal PLL
- Two reference clocks available (19.44 and 51.84 MHz)
- PECL serial interface plus TTL parallel interface
- Single +5 V power supply
- Directly connectable to ATM network termination controller (MB86683 NTC)
- Power save mode with no signal
- Low power consumption (about 0.3 W), wide operating temperature range (–40°C to +85°C)
- High-speed bipolar technology

■ PRODUCT SERIES

Part number	Function	Serial data transmission rate	Transmission code	Transmission medium	Power consumption
MB582A	Transmitter	155.52 Mbps	NRZ	Optical, UTP5	0.25 W
MB583A	Receiver	155.52 Mbps	NRZ	Optical, UTP5	0.3 W

■ PACKAGE

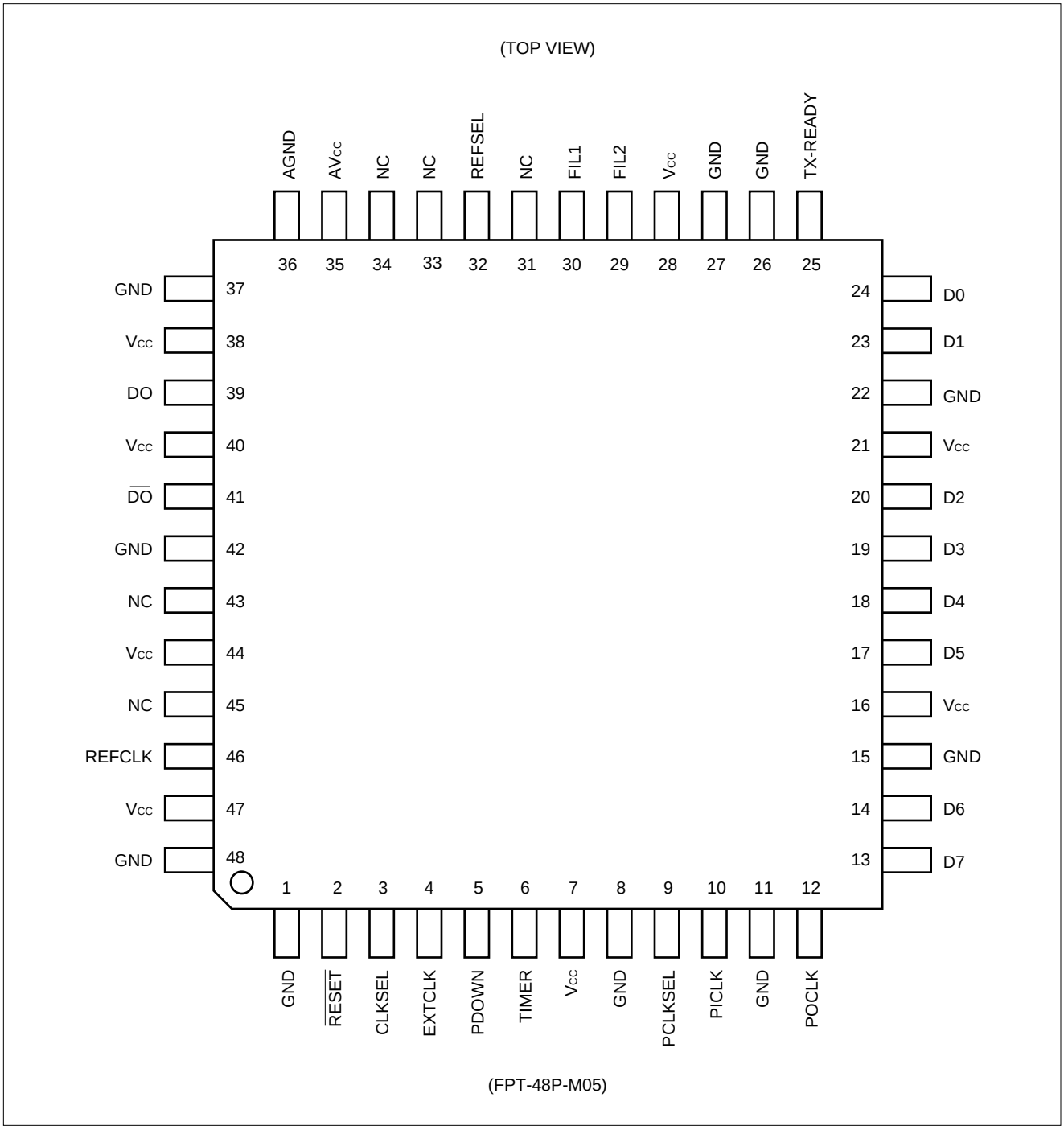
48 pin Plastic LQFP



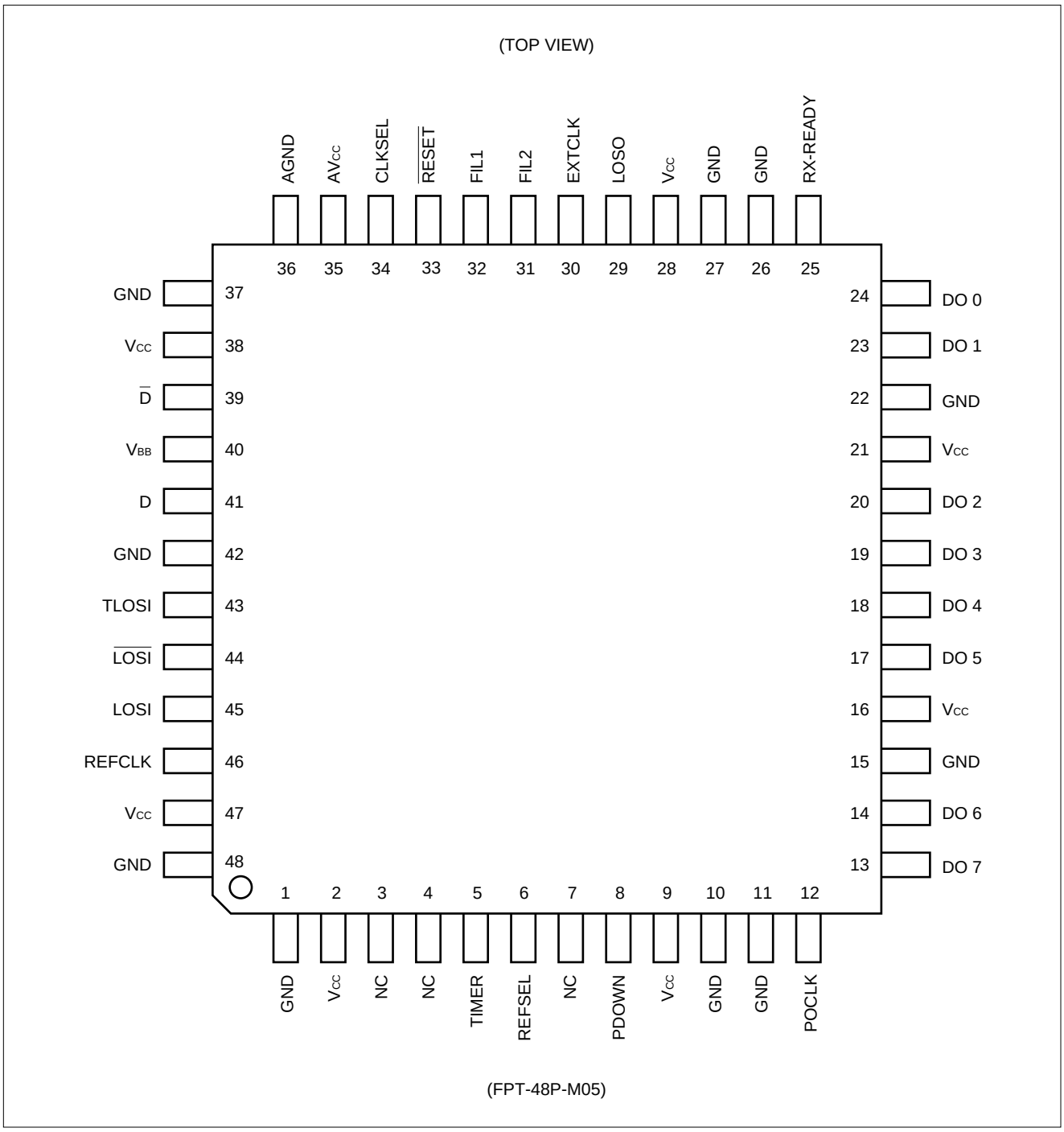
(FPT-48P-M05)

■ PIN ASSIGNMENTS

- **MB582A (transmitter)**



- **MB583A (receiver)**



■ PIN DESCRIPTION

- **MB582A (Transmitter)**

Pin no.	Symbol	Pin name	I/O interface (speed)	Function
24, 23 20 to 17, 14,13	D0 to D7	Parallel data input	TTL input <19.44 Mbyte/s>	**Parallel data input pins:** Parallel data D0 to D7 are fetched at the rising edge of the PICLK pulse or by the internal parallel clock.
10	PICLK	Parallel clock input	TTL input <19.44 MHz>	**Clock input pin for parallel data fetching:** Parallel data D0 to D7 are fetched at the rising edge of the PICLK pulse. This pin is used for the clock synthesizer. Connect a stable oscillator (such as a crystal oscillator within ±20 ppm) to this pin. This pin is used when PCLKSEL = “0”. This pin can’t be used when REFSEL = “0”.
9	PCLKSEL	Parallel clock selection	TTL input <0 or 1>	**Clock selection pin for parallel data fetching:** The internal parallel clock and PICLK are selected when this pin inputs “1” and “0,” respectively. Also, this pin is used to select the reference clock for the clock synthesizer. REFCLK and PICLK are selected when this pin inputs “1” and “0”, respectively.
46	REFCLK	Reference clock input	TTL input <19.44 or 51.84 MHz>	**Reference clock input pin:** This pin is used for the PLL circuit in the clock synthesizer. Connect a stable oscillator (such as a crystal oscillator within ±20 ppm) to this pin. One of two reference clocks can be selected. This pin is used when PCLKSEL = “1”.
32	REFSEL	Reference clock selection	TTL input <0 or 1>	**Reference clock selection pin:** The 19.44- and 51.84-MHz reference clocks are selected when this pin inputs “1” and “0,” respectively.
4	EXTCLK	External clock input	PECL input <up to 155.52 MHz>	**Single PECL input pin:** This pin inputs a high-frequency external clock signal to execute an 8-to-1 multiplexer function independent of the clock synthesizer. In this case, the operating frequency is free and may be up to 155.52 MHz. This pin is used when CLKSEL = “0”.

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Pin no.	Symbol	Pin name	I/O interface (speed)	Function
3	CLKSEL	Clock selection	TTL input <0 or 1>	**Clock selection pin:** The clock generated by the clock synthesizer and the EXTCLK clock are selected when this pin inputs "1" and "0," respectively.
2	$\overline{\text{RESET}}$	Reset input		**Asynchronous reset input pin:** This pin is used to initialize the internal state. The internal circuit is reset when this pin inputs "0". Upon reset, the TX-READY and POCLK pins output Low-level signals. Also, the serial data output pins DO and $\overline{\text{DO}}$ output Low- and High-level signals, respectively. The device must be reset when the power is turned on. For details, see "POWER-ON RESET,P17."
5	PDOWN	Power down	TTL input <0 or 1>	**Sleep mode pin:** The circuit supply current is reduced to about 1/3 of normal level when this pin inputs "1." When it inputs "0," the circuit restores normal operation. In sleep mode, the TX-READY and DO pins output Low-level signals; the $\overline{\text{DO}}$ and POCLK pins output High-level signals. For details on sleep mode, see "USING SLEEP MODE, P19."
39 41	DO $\overline{\text{DO}}$	Serial data output	PECL output <155.52 Mbps>	**Serial data output pins:** These pins output NRZ-coded serial data converted from parallel data in the order of D7 to D0.
12	POCLK	Parallel clock output	TTL output <19.94 MHz>	**Parallel clock output pin:** This pin outputs a parallel clock synchronized with REFLCK. This output pin can be connected to the controller (MB86683 NTC).
25	TX-READY	Ready output	TTL output <L or H>	**Asynchronous READY output pin:** This pin indicates whether the MB582 is ready. The pin outputs the High-level signal when the device is in the ready state. The pin does not indicate the ready state when; the PICLK pulse is not input while PCLKSEL = "0" (selecting PICLK for the parallel clock), $\overline{\text{RESET}}$ = "0" (for reset operation), PDOWN = "1" (for sleep mode), or the PLL circuit in the clock synthesizer is not locked.

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Pin no.	Symbol	Pin name	I/O interface (speed)	Function
6	TIMER	Timer	—	**Timer pin:** This pin can be used for automatic power-on reset by connecting a 4.7 µF capacitor between this pin and the GND pin. Be sure to leave this pin open when not in use. The device must be reset when the power is turned on. The power-on reset can take place automatically only by connecting the capacitor to this pin. For details, see "POWER-ON RESET, P17."
30 29	FIL1 FIL2	External capacitor		**External capacitor connection pins:** A 1 nF capacitor is connected between these pins. This capacitor is the filter capacitor for the clock synthesizer.
31, 33, 34, 43, 45	NC	Unused pin		Leave these pins open.
1, 8, 11, 15, 22, 26, 27, 37, 42, 48	GND	Digital GND	—	**Digital GND pins:** Connect bypass capacitors between these pins and the digital V_{CC} pins.
7, 16, 21, 28, 38, 40, 44, 47	V_{CC}	Digital V_{CC}		**Digital V_{CC} pins:** Connect bypass capacitors between these pins and the digital GND pins.
36	AGND	Analog GND		**Analog GND pin:** Connect bypass capacitors between this pin and the AV_{CC} (analog V_{CC}) pin.
35	AV_{CC}	Analog V_{CC}		**Analog V_{CC} pin:** Connect bypass capacitors between this pin and the AGND (analog GND) pin.

- **MB583A (Receiver)**

Pin no.	Symbol	Pin name	I/O interface (speed)	Function
41 39	D $\overline{D}$	Serial data input	PECL input <155.52 Mbps>	**Serial data input pins:** These pins input NRZ-coded data at 155.52 Mbps.
45 44	LOSI $\overline{LOSI}$	Loss input	PECL input <0 or 1>	**Loss input pins:** When LOSI = "1" and $\overline{LOSI}$ = "0," the input serial data is regarded as being lost; the RX-READY and LOSO pins output Low- and High-level signals, respectively. Since the LOSI and $\overline{LOSI}$ pins are both connected to the reference voltage via an internal high resistor, single input is allowed with either of the pins open. These pins are used when TLOSI = GND.
43	TLOSI	Loss input	TTL input <0 or 1>	**Loss input pin:** When this pin inputs "1," the input serial data is regarded as being lost; the LOSO pin outputs the High-level signal. This pin is used when LOSI = GND and $\overline{LOSI}$ = Open.
46	REFCLK	Reference clock input	TTL input <19.44 or 51.84 MHz>	**Reference clock input pin:** This pin is used for the PLL circuit in the clock recovery unit. Connect a stable oscillator (such as a crystal oscillator within ±20 ppm) to this pin. One of two reference clocks can be selected.
6	REFSEL	Reference clock selection	TTL input <0 or 1>	**Reference clock selection pin:** The 19.44- and 51.84-MHz reference clocks are selected when this pin inputs "1" and "0," respectively.
30	EXTCLK	External clock input	PECL input <up to 155.52 MHz>	**Single PECL input pin:** This pin inputs a high-frequency external clock signal to execute an 1-to-8 demultiplexer function independent of the clock recovery unit. In this case, the operating frequency is free and may be up to 155.52 MHz. This pin is used when CLKSEL = "0".
34	CLKSEL	Clock selection	TTL input <0 or 1>	**Clock selection pin:** The clock generated by the clock recovery unit and the EXTCLK clock are selected when this pin inputs "1" and "0," respectively.
33	$\overline{RESET}$	Reset input	TTL input <0 or 1>	**Asynchronous reset input pin:** This pin is used to initialize the internal state. The internal circuit is reset when this pin inputs "0". Upon reset, the RX-READY, POCLK, and DO0 to DO7 pins output Low-level signals. The device must be reset when the power is turned on. For details, see "POWER-ON RESET,P17."

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Pin no.	Symbol	Pin name	I/O interface (speed)	Function
8	PDOWN	Power down	TTL input <0 or 1>	**Sleep mode pin:** When this pin inputs “1,” the MB583A enters the sleep mode. Actual sleep operation is performed to reduce the circuit supply current to 1/3 of normal level after serial data input of “0” or “1” remains unchanged, or after a loss signal is received. When a serial data signal is received and the loss signal is cleared, the device restores normal circuit operation. Note that, whenever the serial data input is variable in level without being fixed as “1” or “0”, the device will assume that data is being received (the optical module connected to the serial data input may output variable level when the optical signal interrupted). When PDOWN = “0”, the device does not enter the sleep mode regardless of the status of the serial data or loss signals. In sleep state, the RX-READY pin outputs the Low-level signal; the LOSO, POCLK, and DO0 to DO7 pins output High-level signals. For details on the sleep mode, see “USING SLEEP MODE, P19.”
24, 23, 20 to 17, 14, 13	DO0 to DO7	Parallel data output	TTL output <19.44 Mbyte/s>	**Parallel data output pins:** These pins output NRZ-coded parallel data converted from serial data in the order of DO7 to DO0.
12	POCLK	Parallel clock output	TTL output <19.44 MHz>	**Parallel clock output pin:** This pin outputs a parallel clock synchronized with serial data. This output pin can be connected to the controller (MB86683 NTC). If no serial data is input when PDOWN = “0” (sleep mode off) or a loss signal is received, this pin serves as a parallel clock output synchronized with REFCLK. If no serial data is input when PDOWN is “1” (sleep mode on) or a loss signal is received, the device enters the sleep state and this pin outputs the High-level signal. Note that, whenever the serial data input is variable in level without being fixed as “1” or “0,” the device will assume that data is being received (the optical module connected to the serial data input may output variable level when the optical signal interrupted).

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Pin no.	Symbol	Pin name	I/O interface (speed)	Function
29	LOSO	Loss output	TTL output <L or H>	**Asynchronous Loss output pin:** This pin outputs the High-level signal after serial data input of “0” or “1” remains unchanged or on reception of a loss signal. Note that, whenever the serial data input is variable in level without being fixed as “1” or “0,” the device will assume that data is being received (the optical module connected to the serial data input may output variable level when the optical signal interrupted). This output pin can be connected to the controller (MB86683 NTC).
25	RX-READY	Ready output	TTL output <L or H>	**Asynchronous READY output pin:** This pin indicates whether the MB583A is ready. The pin outputs the High-level signal when the device is in the ready state. The pin does not indicate the ready state when; serial data input of “0” or “1” remains unchanged, on reception of a loss signal, $\overline{\text{RESET}}$ = “0,” or the PLL circuit in the clock recovery unit is not locked.
40	V_{BB}	Reference voltage output	—	**Reference voltage output pin:** For single input of serial data, connect the VBB and $\overline{\text{D}}$ pins using a resistor. For differential input of serial data, leave this pin open.
5	TIMER	Timer		**Timer pin:** This pin can be used for automatic power-on reset by connecting a 4.7 μF capacitor between this pin and the GND pin. Be sure to leave this pin open when not in use. The device must be reset when the power is turned on. The power-on reset can take place automatically only by connecting the capacitor to this pin. For details, see “POWER-ON RESET, P17.”
32 31	FIL1 FIL2	External capacitor		**External capacitor connection pins:** A 1 nF capacitor is connected between these pins. This capacitor is the filter capacitor for the clock recovery.
3, 4, 7	NC	Unused pin		Leave these pins open.

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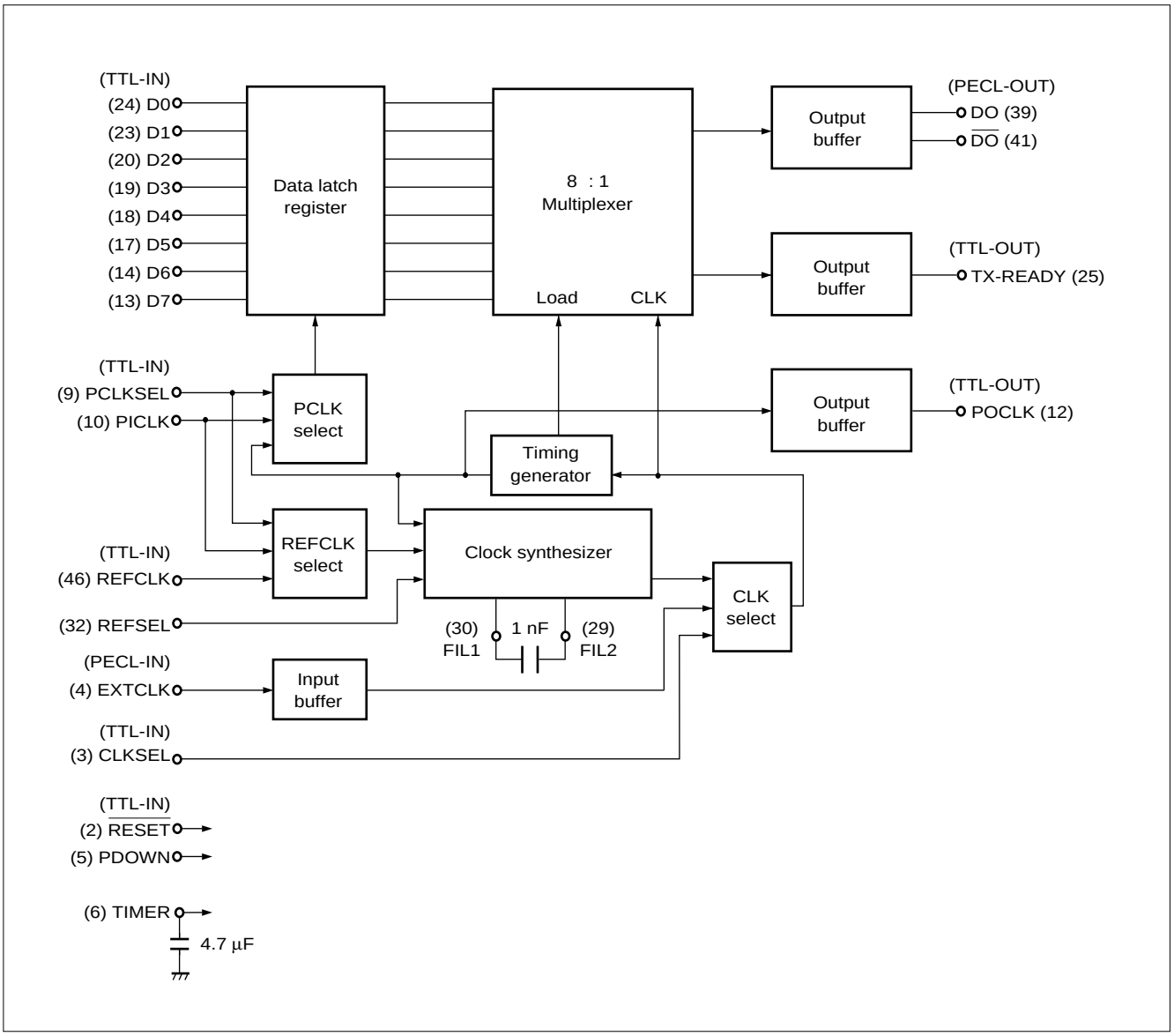
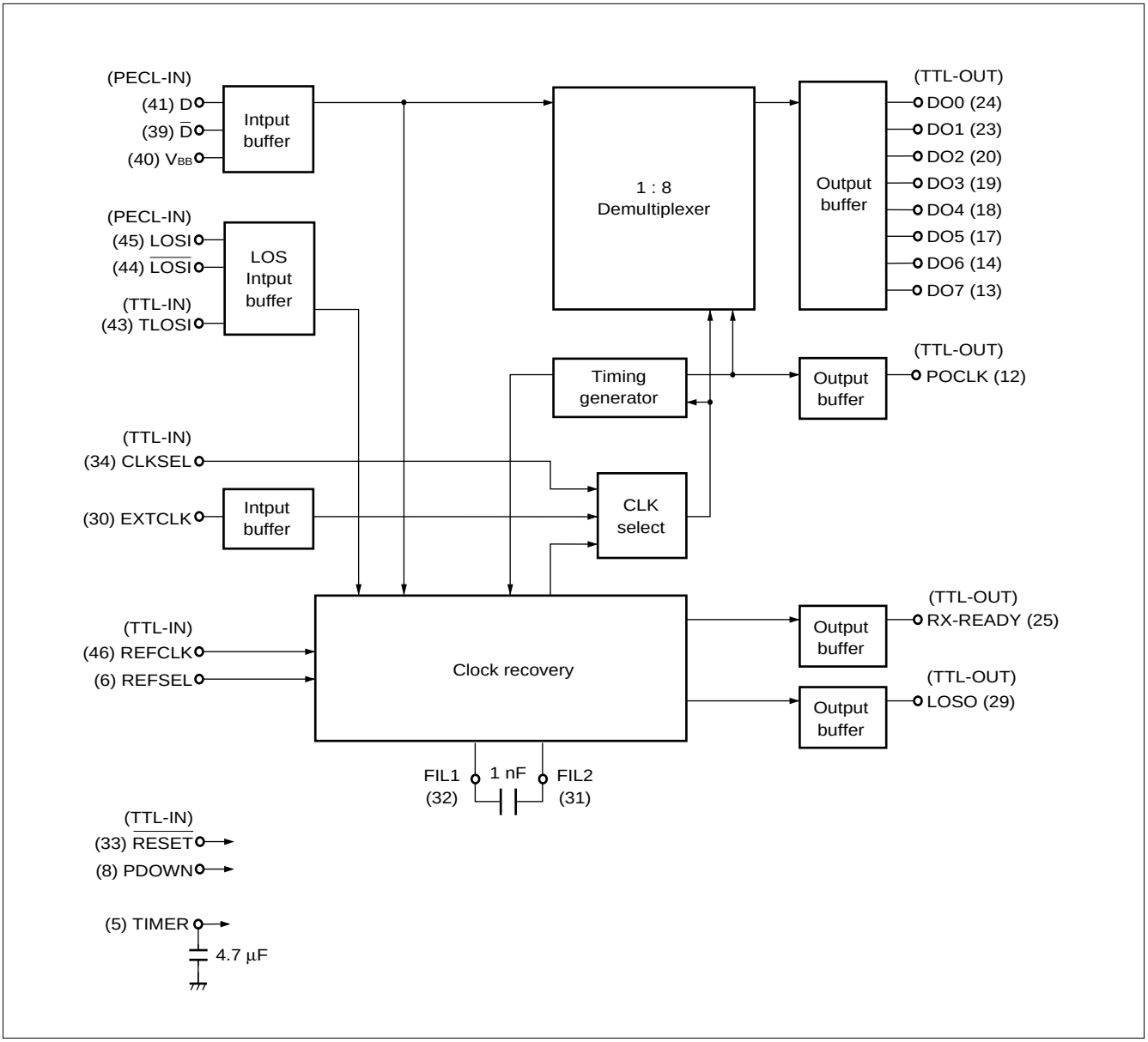
Pin no.	Symbol	Pin name	I/O interface (speed)	Function
1, 10, 11, 15, 22, 26, 27, 37, 42, 48	GND	Digital GND	—	**Digital GND pins:** Connect bypass capacitors between these pins and the digital V_{CC} pins.
2, 9, 16, 21, 28, 38, 47	V_{CC}	Digital GND		**Digital V_{CC} pins:** Connect bypass capacitors between these pins and the digital GND pins.
36	AGND	Analog GND		**Analog GND pin:** Connect bypass capacitors between this pin and the AV_{CC} (analog V_{CC}) pin.
35	AV_{CC}	Analog V_{CC}		**Analog V_{CC} pin:** Connect bypass capacitors between this pin and the AGND (analog GND) pin.

■ BLOCK DIAGRAMS

- **MB582A (Transmitter)**



- **MB583A (Receiver)**



■ FUNCTIONS

(1) MB582A (Transmitter)

- **Reference clock function**

PCLKSEL	REFSEL	Reference clock terminal	Reference clock frequency
1 (OPEN)	1 (OPEN)	REFCLK	19.44 MHz
	0	REFCLK	51.84 MHz
0	1 (OPEN)	PICLK	19.44 MHz
	0	Prohibit	—

- **High-frequency clock function**

CLKSEL	Internal clock
1 (OPEN)	Clock synthesizer
0	EXTCLK

- **Reset function**

$\overline{\text{RESET}}$	Reset
1 (OPEN)	—
0	Reset

- **Parallel clock function**

PCLKSEL	Parallel data input clock
1 (OPEN)	Internal parallel clock (setup/hold time required between POCLK and D0 to D7)
0	PICLK (setup/hold time required between PICLK and D0 to D7)

- **Sleep mode function**

PDOWN	Sleep mode
1	Sleep
0 (OPEN)	Wake-up

- **Ready signal function**

TX-READY	Device state
H	Ready
L	Not ready

The device is not ready when;

- PICLK is not input while PCLKSEL = “0” (selecting PICLK as parallel clock input)
- $\overline{\text{RESET}}$ = “0” (reset operation)
- PDOWN = “1” (sleep state)
- The PLL circuit in the clock synthesizer is not locked (because of the REFCLK frequency not matched, external resistor not connected, etc.)

- **PDOWN and $\overline{\text{RESET}}$ functions**

PDOWN	$\overline{\text{RESET}}$	Sleep mode	TX-READY	DO	$\overline{\text{DO}}$	POCLK
1	X	Sleep	L	L	H	H
0	1	Not sleep	H	Normal operation	Normal operation	Normal operation
	0		L	L	H	L

X: 0 or 1

(2) MB583A (Receiver)

- **Reference clock function**

REFSEL	REFCLK
1 (OPEN)	19.44 MHz
0	51.84 MHz

- **High-frequency clock function**

CLKSEL	Internal clock
1 (OPEN)	Clock recovery
0	EXTCLK

- **Reset function**

$\overline{\text{RESET}}$	Reset
1 (OPEN)	—
0	Reset

- **Loss function**

LOSO	Input serial data
H	Los detection
L	Receive state

LOSI, TLOSI	Input serial data
1	Los detection
0	Receive state

Loss signal selection	Setting conditions
LOSI, $\overline{\text{LOSI}}$ (PECL)	TLOSI = GND (OPEN)
TLOSI (TTL)	LOSI = GND also $\overline{\text{LOSI}}$ = OPEN

LOSO = H when;

- LOSI or TLOSI = “1”
- Input serial data of “0” or “1” remains unchanged.*

* : Note that, whenever the serial data input is variable in level without being fixed as “0” or “1,” the device will assume that data is being received (the optical module connected to the serial data input may output variable level when the optical signal interrupted).

- **Sleep mode function**

PDOWN	Sleep mode
1 (OPEN)	Sleep mode ON
0	Sleep mode OFF

- **Ready signal function**

RX-READY	Device state
H	Ready
L	Not ready

The sleep mode is turned on when;

- Input serial data of “0” or “1” remains unchanged.*
- The loss signal is received.

The device is not ready when;

- Input serial data of “0” or “1” remains unchanged.*
- The loss signal is received.
- $\overline{\text{RESET}}$ = “0” (reset operation)
- The PLL circuit in the clock recovery unit is not locked (because of the REFCLK frequency not matched, external resistor not connected, etc.)

- **Input serial data, PDOWN, RESET, LOSI, and TLOSI functions**

Input serial data	PDOWN	$\overline{\text{RESET}}$	LOSI, TLOSI	Sleep mode	RX-READY	LOSO	DO0 to DO7	POCLK
Receive state	1	1	1	Sleep	L	H	H	H
			0	Not sleep	H	L	Normal operation	Normal operation
		0	1	Sleep	L	H	H	H
			0	Not sleep		L	L	L
	0	1	1	Not sleep	L	H	Undefined	Synchronizing with REFCLK
			0		H	L	Normal operation	Normal operation
		0	1		L	H	L	L
			0			L		
Loss state	1	X	X	Sleep	L	H	H	H
	0	1	X	Not sleep	L	H	Undefined	Synchronizing with REFCLK
		0					L	L

Loss state: Input serial data of “0” or “1” remains unchanged.*

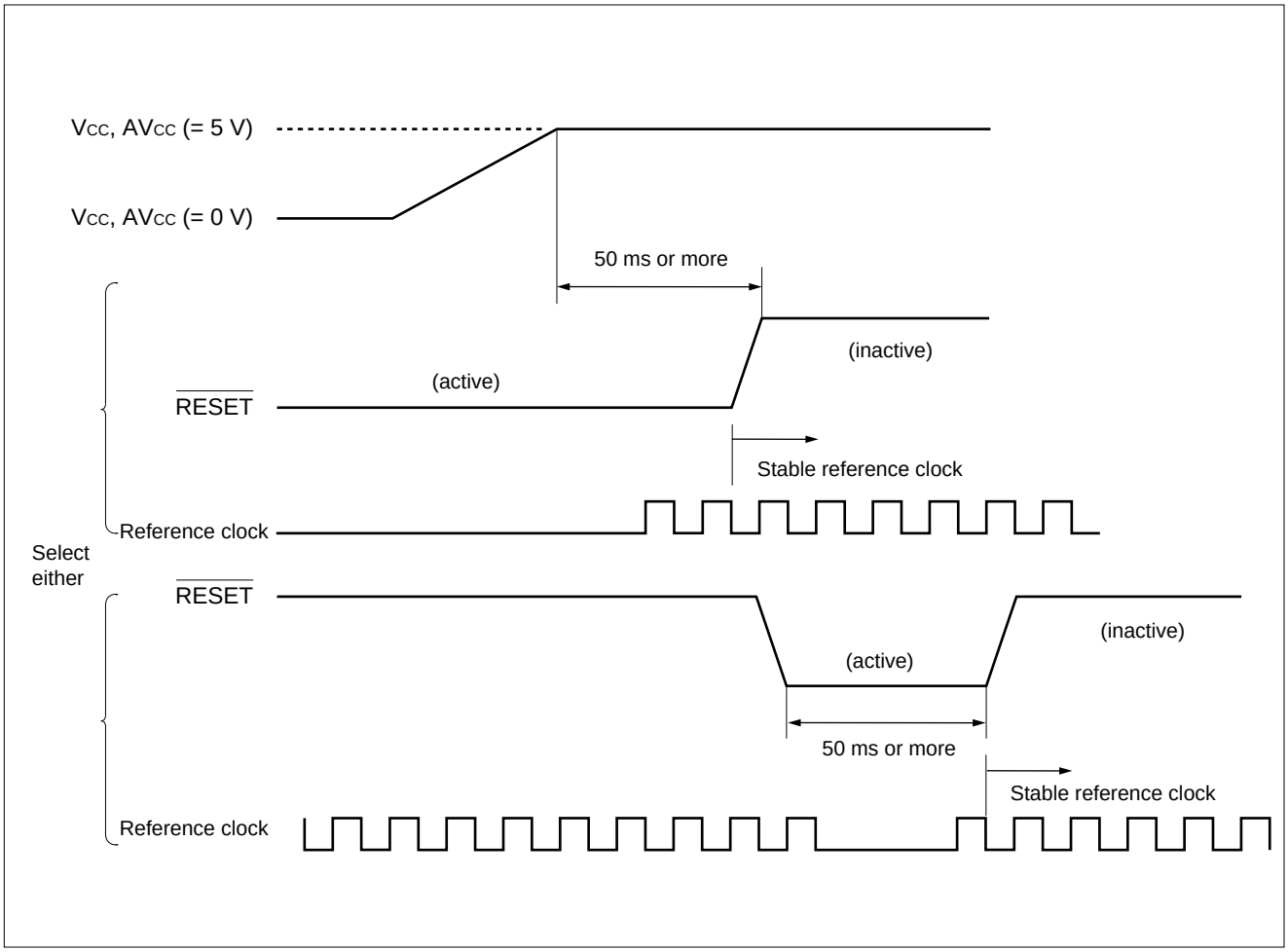
X: 0 or 1

* : Note that, whenever the serial data input is variable in level without being fixed as “0” or “1,” the device will assume that data is being received (the optical module connected to the serial data input may output variable level when the optical signal interrupted).

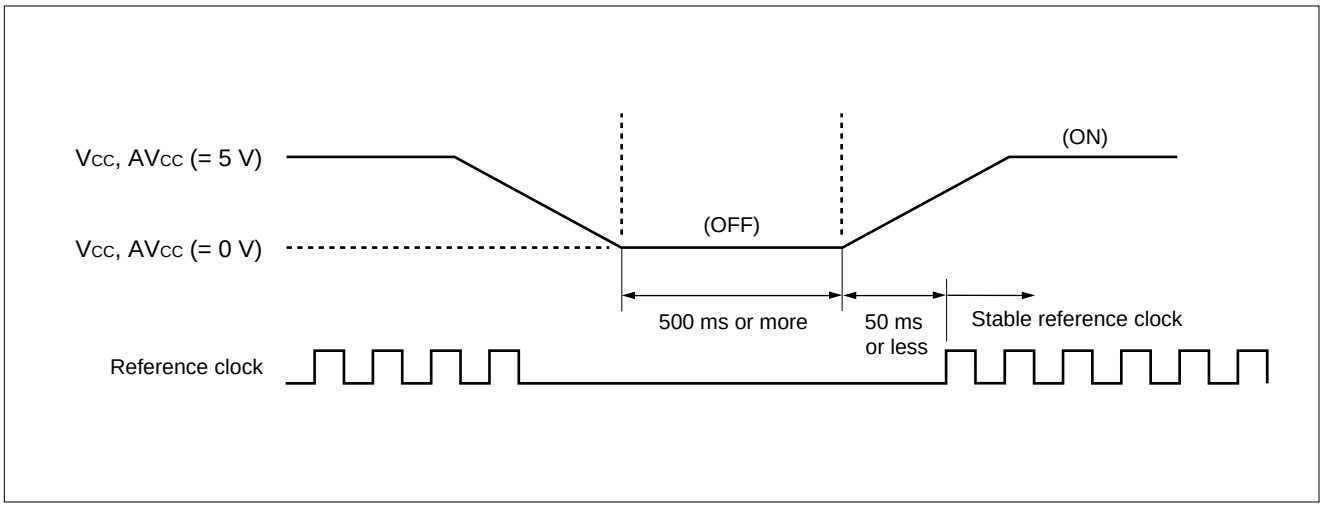
■ POWER-ON RESET

The MB582A and MB583A must be reset when the power is turned on. There are two methods available for resetting each device at power-on. Select the best method.

(1) Apply a reset to the device at power-on, then cancel the reset 50 ms after the V_{CC} and AV_{CC} have reached 5 V or input a reset pulse with a width of 50 ms after they reached 5 V. Note that a stable reference clock signal (REFCLK or PICLK) must be input before the reset is canceled. (See the diagram below.)
This method eliminates the need for connecting an external capacitor to the TIMER pin as described in method (2).
Be sure to leave the TIMER pin open when not in use.



(2) Connect a 4.7 µF external capacitor between the TIMER and GND pins. The capacitor is used for automatic power-on reset.
Whenever the power is recycled, ensure that it remains off for at least 500 ms. (See the diagram below.)
This method allows the $\overline{\text{RESET}}$ signal to be used without considering the restrictions described in method (1).
The $\overline{\text{RESET}}$ pin may be left open.
Note, however, that a stable reference clock signal (REFCLK or PICLK) must be input within 50 ms after power-on.

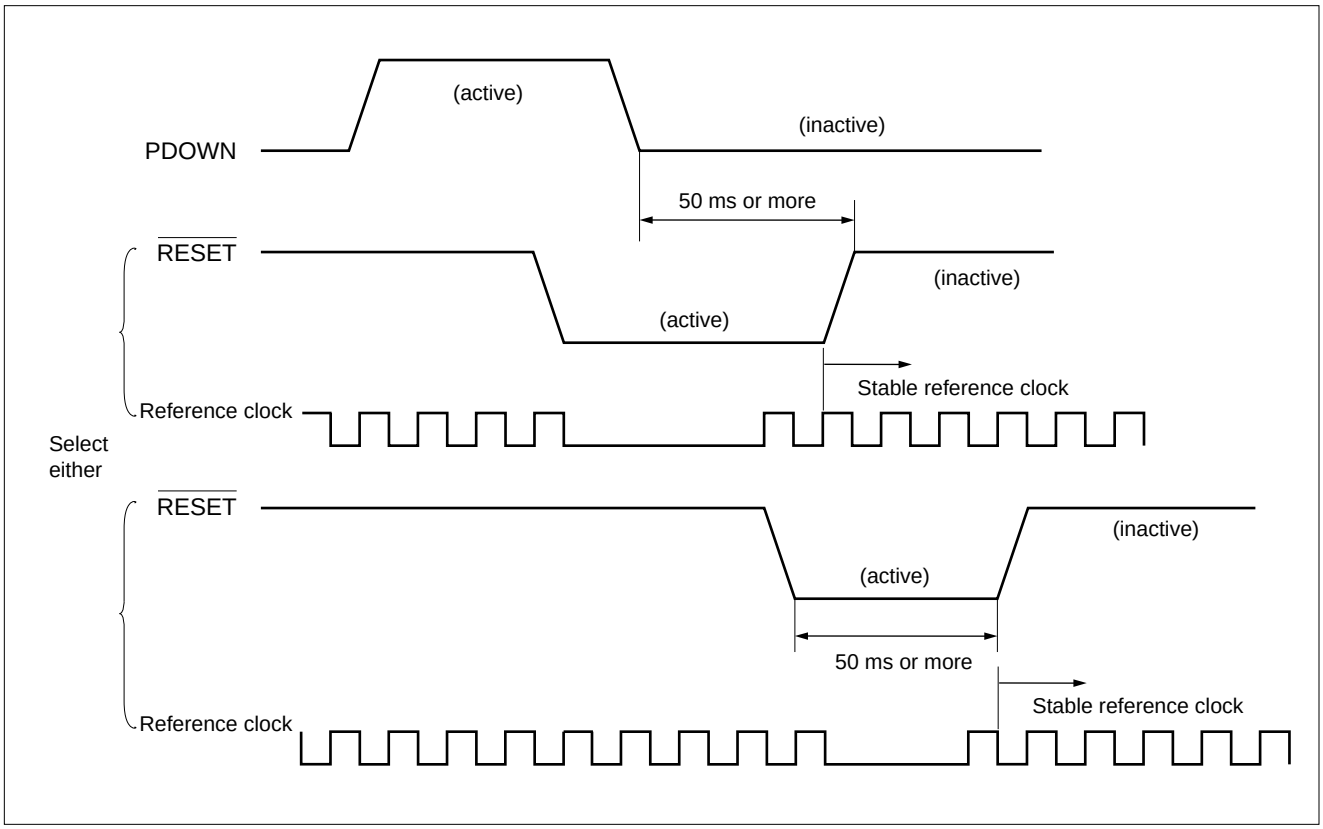


■ USING SLEEP MODE

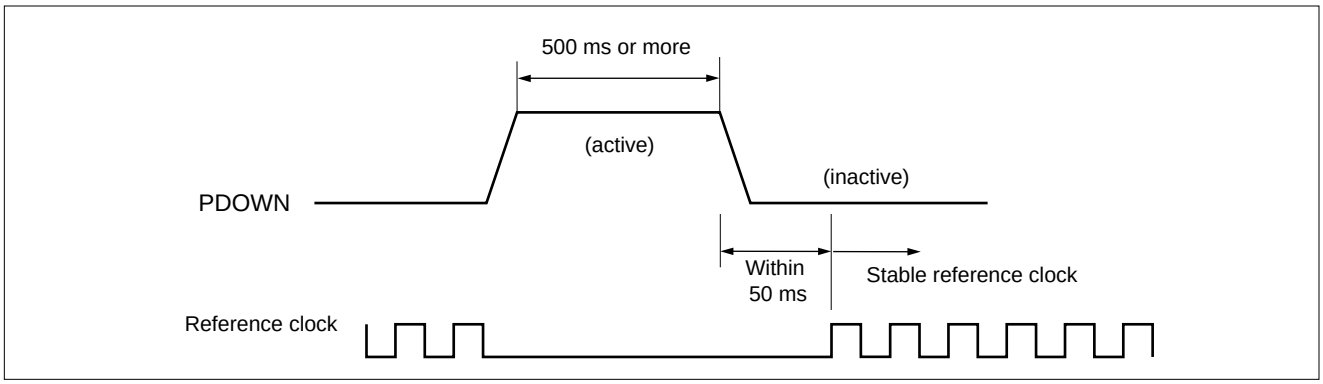
- **Using the MB582A Sleep Mode**

It is necessary to follow either method (1) or (2) when using the sleep mode, otherwise the device will not return to normal operating status.

(1) Apply a reset to the device when it enters sleep mode, then cancel the reset 50 ms after clearing the PDOWN signal or input a reset pulse with a width of 50 ms after clearing the PDOWN signal. Note that a stable reference clock signal (REFCLK or PICLK) must be input before the reset is canceled. (See the diagram below.)
This method eliminates the need for connecting an external capacitor to the TIMER pin as described in method (2).
Be sure to leave the TIMER pin open when not in use.



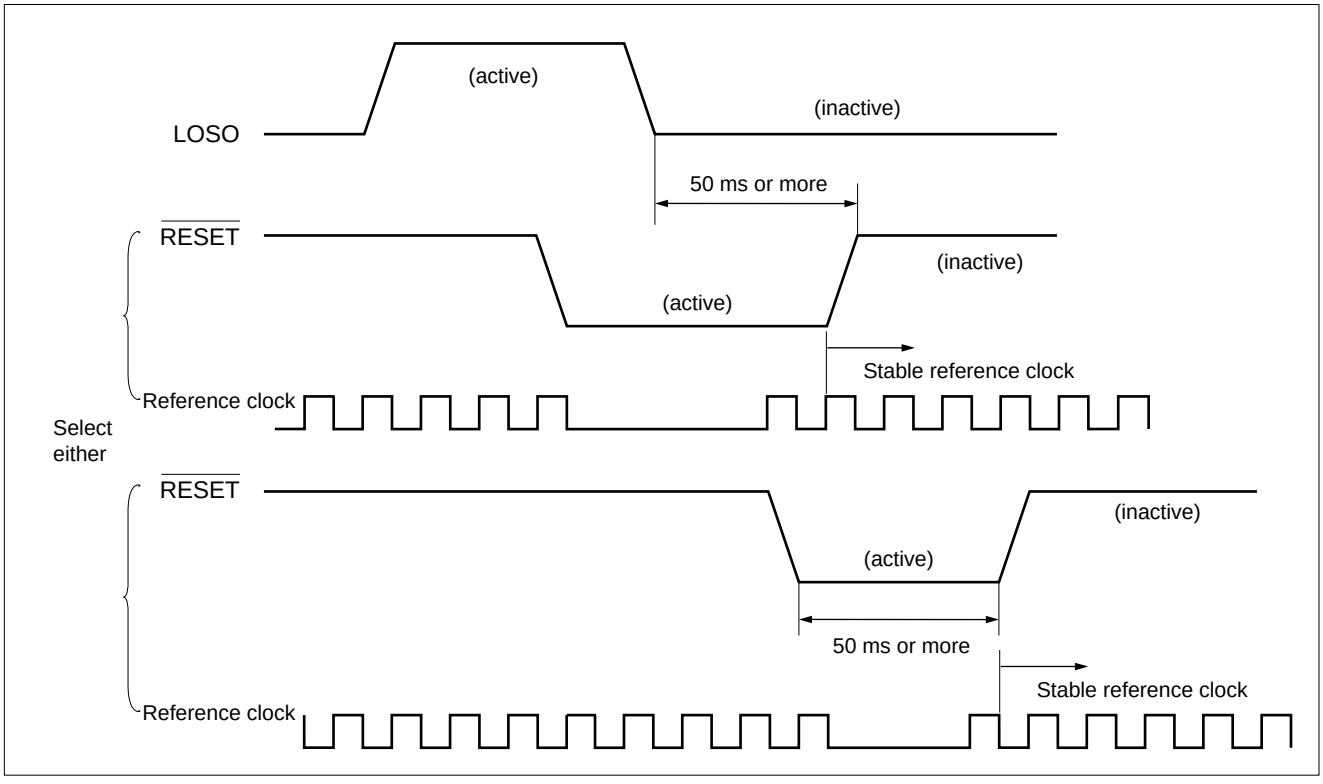
(2) Connect a 4.7 µF external capacitor between the TIMER and GND pins. The capacitor is used for automatically resetting the sleep mode.
Be sure that the PDOWN signal has an active phase of at least 500 ms. (See the diagram below.)
This method allows the $\overline{\text{RESET}}$ signal to be used without considering the restrictions described in method (1).
The $\overline{\text{RESET}}$ pin may be left open.
Note, however, that a stable reference clock signal (REFCLK or PICLK) must be input within 50 ms after the power save mode is canceled (as shown in the following illustration.)



- **Using the MB583A Sleep Mode**

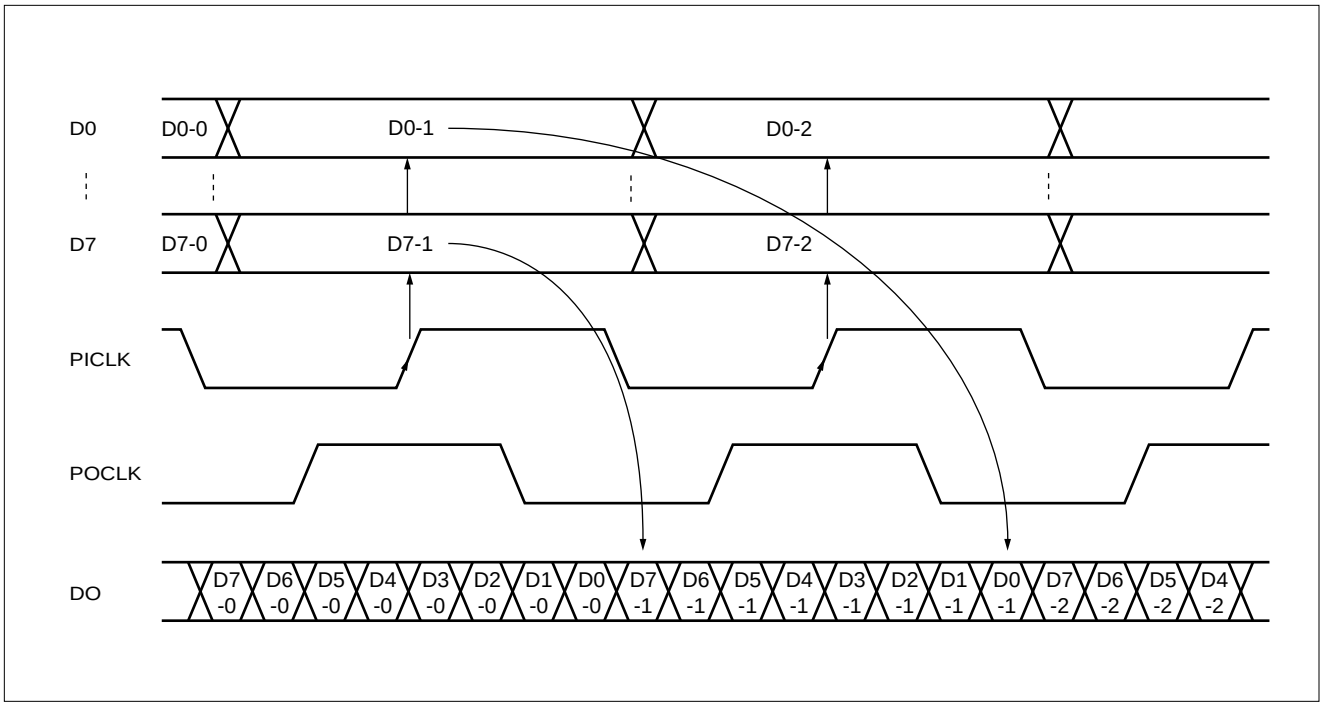
It is necessary to use method (1) when using the sleep mode, otherwise the device will not return to normal operating status.

(1) Apply a reset to the device when the LOSO output goes high (the LOS state detected), then cancel the reset 50 ms after the LOSO output goes low (receive state) or input a reset pulse with a width of 50 ms after the LOSO output changes from high to low. Note that a stable reference clock signal (REFCLK) must be input before the reset is canceled. (See the diagram below.)
Be sure to leave the TIMER pin open when not in use.

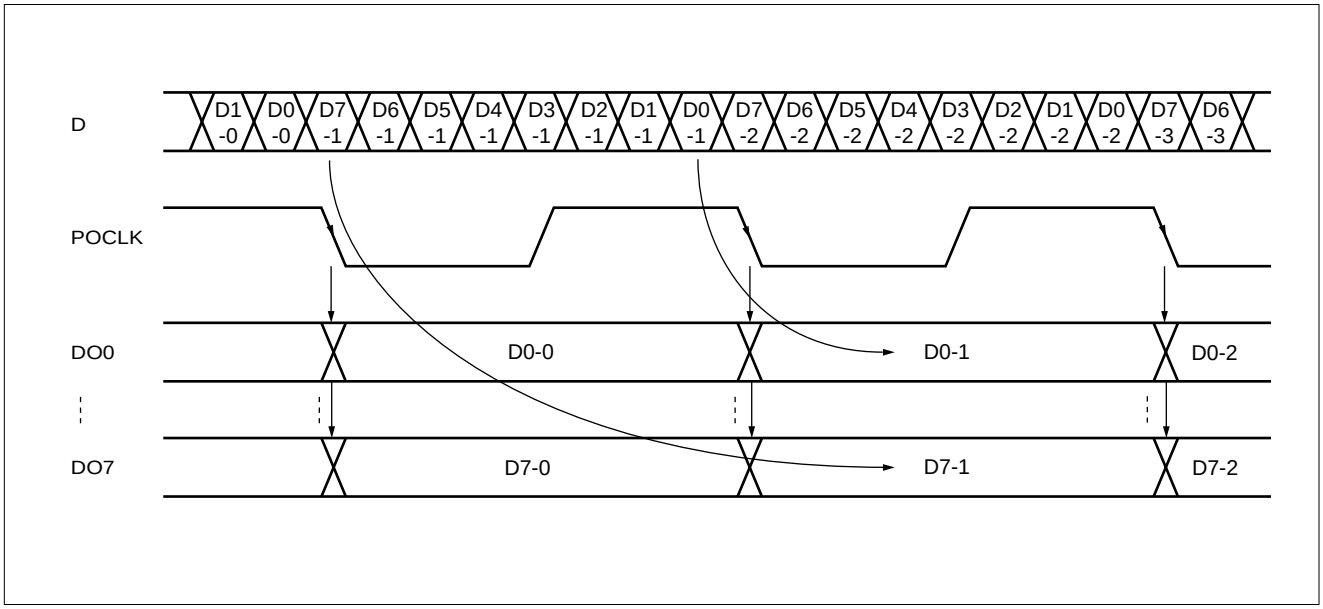


■ TIMING CHARTS

- **MB582A (Transmitter)**



- **MB583A (Receiver)**



■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Power supply voltage*		V_{CC}	0 to 6.0	V
Input voltage*	TTL	V_{IN}	–0.5 to V_{CC}+0.5	V
	PECL	V_{IN}	2.0 to V_{CC}	V
Output voltage*	TTL	V_{OUT}	–0.5 to 5.5	V
Output current	PECL	I_{OUT}	–50	mA
Storage temperature		Tstg	–55 to +150	°C

* : The voltage is based on GND.

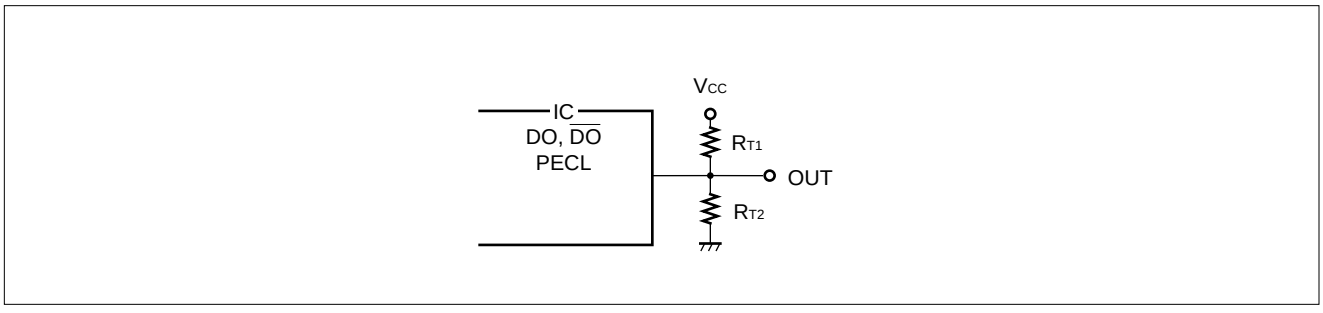
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value	Unit
Power supply voltage*		V_{CC}	5.0 ±5 %	V
High-level output current	TTL	I_{OH}	–1	mA
Low-level output current		I_{OL}	4	mA
DO and $\overline{DO}$ output termination resistors	PECL—V_{CC}	R_{T1}	82	Ω
	PECL—GND	R_{T2}	130	Ω
Operating temperature		Ta	–40 to +85	°C

* : The voltage is based on GND.

- **Connection diagram of PECL output termination resistor**



■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

- **MB582A (transmitter)**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions		Value			Unit
					Min.	Typ.*1	Max.	
TTL input	High-level input voltage	V_{IH}	—		2.0	—	—	V
	Low-level input voltage	V_{IL}	—		—	—	0.8	V
	Input clamp voltage	V_{IC}	V_{CC} = 4.75 V, I_I = –18 mA		–1.5	—	—	V
	High-level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.4 V		—	—	500	µA
	Low-level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.5 V		–500	—	—	µA
TTL output	High-level output voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = –1 mA		2.4	—	—	V
	Low-level output voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 4 mA		—	—	0.5	V
	Output short-circuit current*2	I_{OS}	V_{CC} = 5.25 V, V_O = 0 V		–150	—	—	mA
Single PECL input (EXTCLK)	High-level input voltage	V_{IH}	—		V_{CC} – 1.165	—	V_{CC} – 0.72	V
	Low-level input voltage	V_{IL}	—		V_{CC} – 1.95		V_{CC} – 1.475	V
	High-level input current	I_{IH}	V_I = V_{CC} – 0.72 V		—	—	200	µA
	Low-level input current	I_{IL}	V_I = V_{CC} – 1.95 V		–200	—	—	µA
	Input open-circuit voltage	V_{IO}	—		V_{CC} – 1.26	V_{CC} – 1.32	V_{CC} – 1.38	V
PECL output (DO, $\overline{DO}$)	High-level output voltage	V_{OH}	Output load: 82 Ω to V_{CC} 130 Ω to GND	Ta = –40°C	V_{CC} – 1.15	—	V_{CC} – 0.89	V
				Ta = 0°C	V_{CC} – 1.09	—	V_{CC} – 0.84	V
				Ta = +25°C	V_{CC} – 1.05	V_{CC} – 0.92	V_{CC} – 0.81	V
				Ta = +75°C	V_{CC} – 0.99	—	V_{CC} – 0.735	V
				Ta = +85°C	V_{CC} – 0.98	—	V_{CC} – 0.72	V

*1: Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

*2: The output short-circuit duration must not exceed 1 second. More than one output must not be short-circuited at the same time.

(Continued)

(Continued)

Parameter		Symbol	Conditions		Value			Unit
					Min.	Typ.*1	Max.	
PECL output (DO, $\overline{DO}$)	Low-level output voltage	V_{OL}	Output load: 82 Ω to V_{CC} 130 Ω to GND	Ta = –40°C	V_{CC} – 1.15	—	V_{CC} – 1.63	V
				Ta = 0°C	V_{CC} – 1.09	—	V_{CC} – 1.63	V
				Ta = +25°C	V_{CC} – 1.05	V_{CC} – 0.92	V_{CC} – 1.63	V
				Ta = +75°C	V_{CC} – 0.99	—	V_{CC} – 1.60	V
				Ta = +85°C	V_{CC} – 0.98	—	V_{CC} – 1.595	V
Supply current	During operation	I_{CC}	V_{CC} = 5.25 V, I/O = Open		—	50	80	mA
	Sleep state	I_{CCD}	V_{CC} = 5.25 V, PDOWN = "1" Other I/O pins = Open		—	15	40	mA
PECL output current (DO + $\overline{DO}$)	During operation	I_{O1}	V_{CC} = 5.25 V Output load: 82 Ω to V_{CC} 130 Ω to GND		–35	–24	—	mA
	Sleep state	I_{OD1}			–35	–24	—	mA

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

• **MB583A (receiver)** (V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*1	Max.	
TTL input	High-level input voltage	V_{IH}	—	2.0	—	—	V
	Low-level input voltage	V_{IL}	—	—	—	0.8	V
	Input clamp voltage	V_{IC}	V_{CC} = 4.75 V, I_I = –18 mA	–1.5	—	—	V
	High-level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.4 V	—	—	500	µA
	Low-level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.5 V	–500	—	—	µA
TTL output	High-level output voltage	V_{OH}	V_{CC} = 4.75 V, I_{OH} = –1 mA	2.4	—	—	V
	Low-level output voltage	V_{OL}	V_{CC} = 4.75 V, I_{OL} = 4 mA	—	—	0.5	V
	Output short-circuit current*2	I_{OS}	V_{CC} = 5.25 V, V_O = 0 V	–150	—	—	mA
Differential PECL input (D, $\overline{D}$, LOSI, $\overline{LOSI}$)	High-level input voltage	V_{IH}	—	—	—	V_{CC} – 0.72	V
	Low-level input voltage	V_{IL}	—	V_{CC} – 1.95	—	—	V
	Differential input voltage	V_{dif}	V_{IH} – V_{IL}	0.1	—	1.2	V
	High-level input current	I_{IH}	V_I = V_{CC} – 0.72 V	—	—	200	µA
	Low-level input current	I_{IL}	V_I = V_{CC} – 1.95 V	–200	—	—	µA
Single PECL input (EXTCLK, LOSI, $\overline{LOSI}$)	High-level input voltage	V_{IH}	—	V_{CC} – 1.165	—	V_{CC} – 0.72	V
	Low-level input voltage	V_{IL}	—	V_{CC} – 1.95	—	V_{CC} – 1.475	V
	High-level input current	I_{IH}	V_I = V_{CC} – 0.72 V	—	—	200	µA
	Low-level input current	I_{IL}	V_I = V_{CC} – 1.95 V	–200	—	—	µA
	Input open-circuit voltage	V_{IO}	—	V_{CC} – 1.26	V_{CC} – 1.32	V_{CC} – 1.38	V

*1: Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

*2: The output short-circuit duration must not exceed 1 second. More than one output must not be short-circuited at the same time.

(Continued)

(Continued)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*1	Max.	
V_{BB} output	Reference voltage	V_{BB}	—	V_{CC} – 1.26	V_{CC} – 1.32	V_{CC} – 1.38	V
	During operation	I_{CC}	V_{CC} = 5.25 V, PDOWN = "0" Other I/O pins = Open	—	60	110	mA
Supply current	Sleep state	I_{CCD}	V_{CC} = 5.25 V, PDOWN = "0" Other I/O pins = Open	—	20	50	mA

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

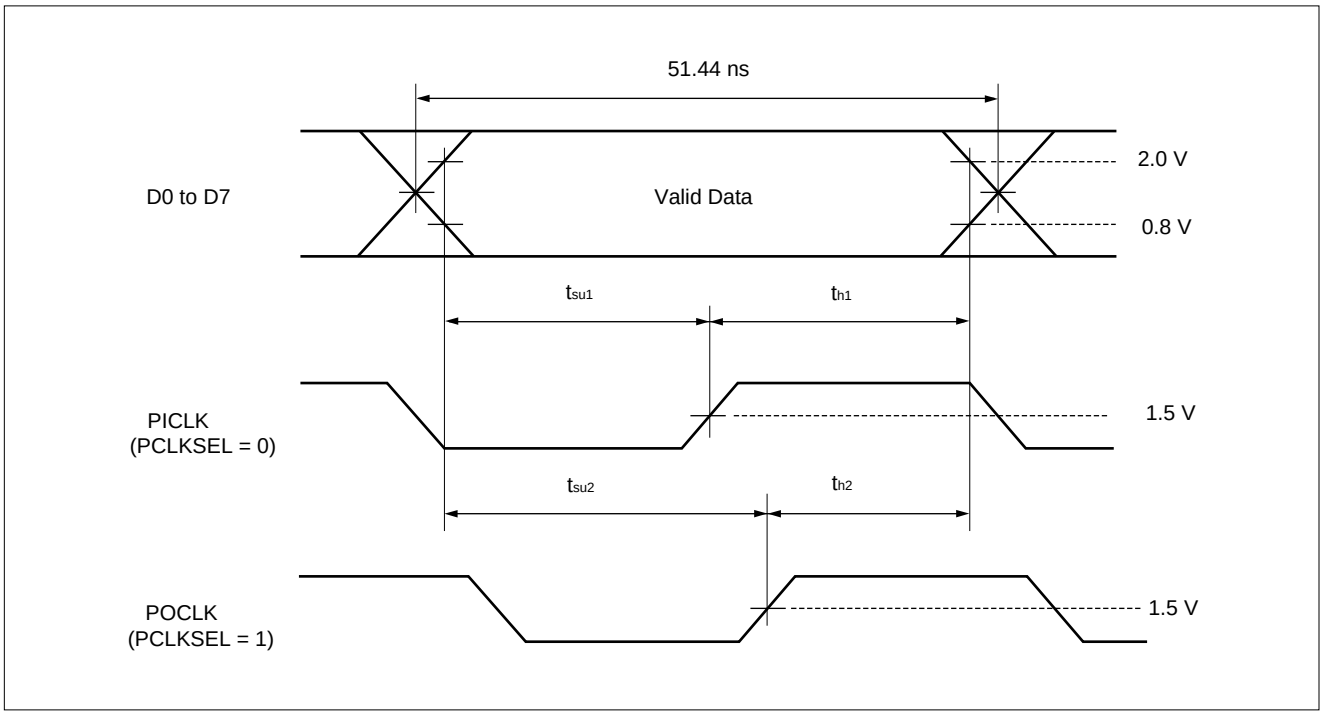
2. AC Characteristics

(1) MB582A (transmitter)

- **Parallel clock input and parallel data input timings**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

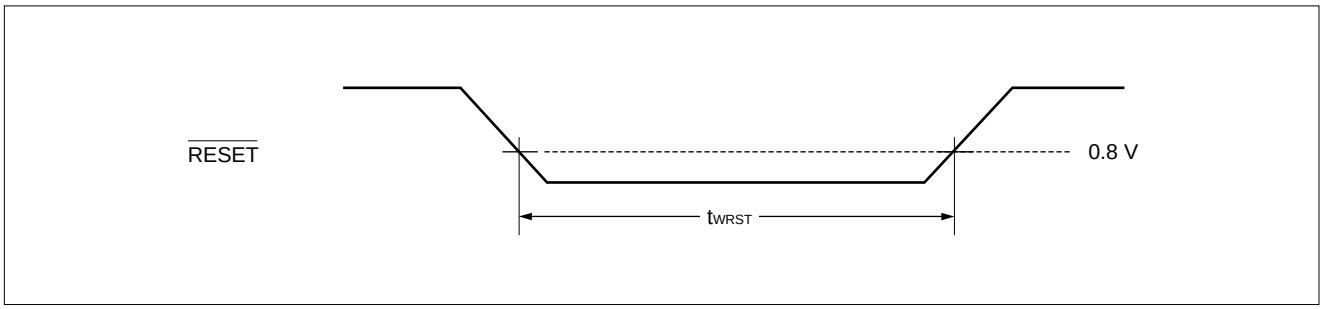
Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
PICLK ↔ D0 to D7	Setup time	t_{su1}	PCLKSEL = “0”	5.0	—	—	ns
	Hold time	t_{h1}		5.0	—	—	ns
POCLK ↔ D0 to D7	Setup time	t_{su2}	PCLKSEL = “1”	5.0	—	—	ns
	Hold time	t_{h2}		5.0	—	—	ns



- **Reset input pulse width**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
$\overline{\text{RESET}}$	Pulse width	t_{WRST}	—	100	—	—	ns

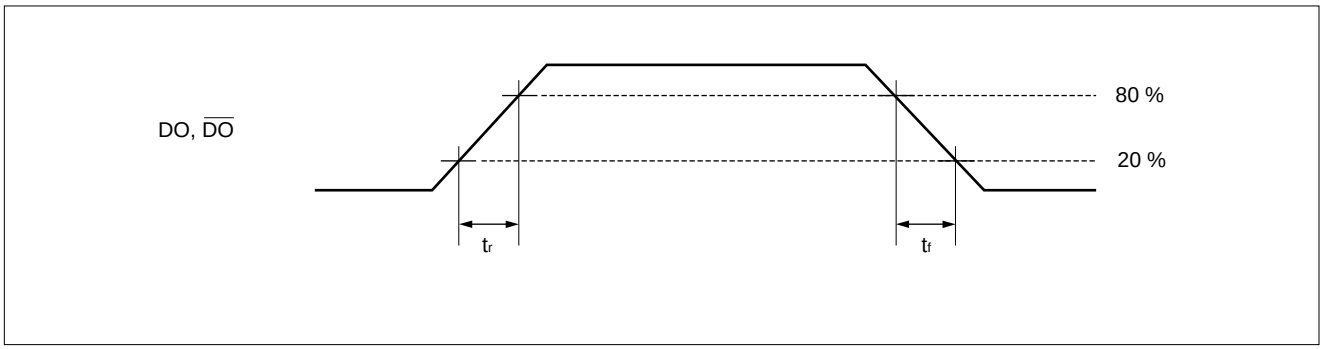


- **PECL output waveform**

(V_{CC} = +5.0 V ±5.0 %,Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
DO, $\overline{\text{DO}}$	Rise time	t_r	20 % –80 % Output load: 82 Ω to V_{CC} 130 Ω to GND	—	0.7	—	ns
	Fall time	t_f		—	0.7	—	ns

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

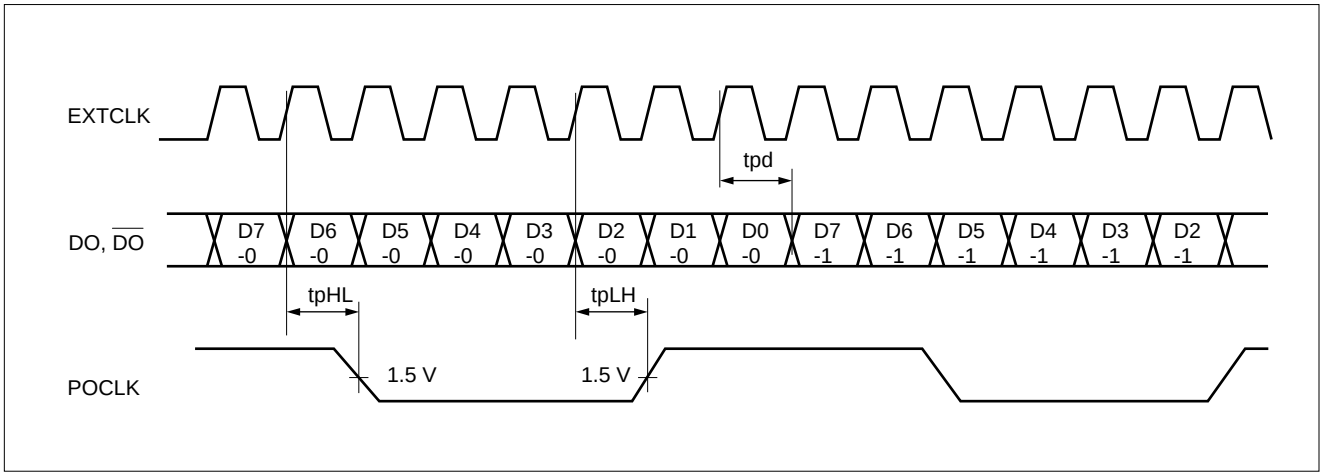


- **External serial clock input timing**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
EXTCLK → POCLK	Delay	tpHL	CLKSEL = “0”	—	12.0	—	ns
EXTCLK → POCLK	Delay	tpHL	CLKSEL = “0”	—	12.0	—	ns
EXTCLK → DO, $\overline{DO}$	Delay	tpd	CLKSEL = “0”	—	6.0	—	ns

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.



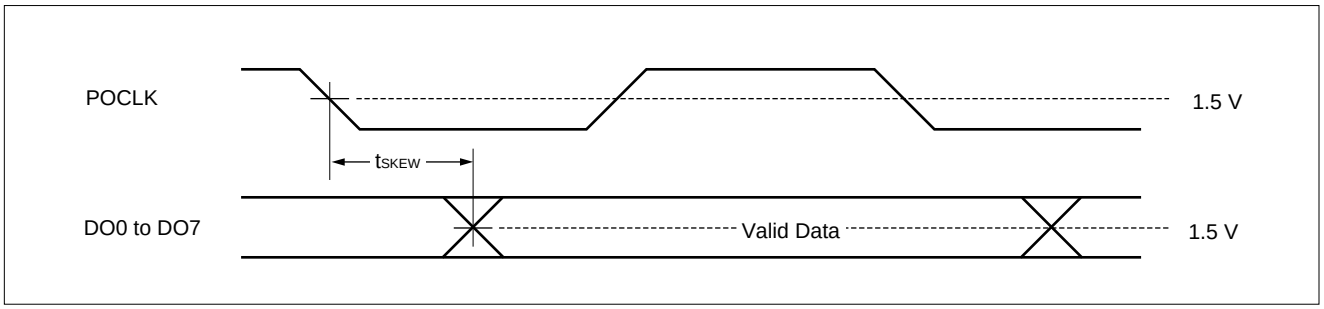
(2) MB583A (receiver)

- **Parallel clock output and parallel data output timings**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
POCLK → DO0 to DO7	Skew	t_{SKEW}	—	–5.0	0	5.0	ns

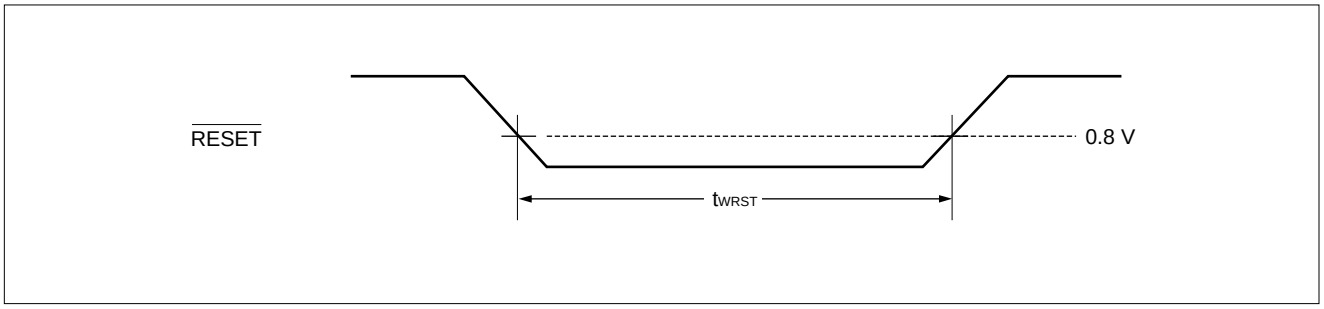
* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C



- **Reset input pulse width**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
$\overline{\text{RESET}}$	Pulse width	t_{WRST}	—	100	—	—	ns

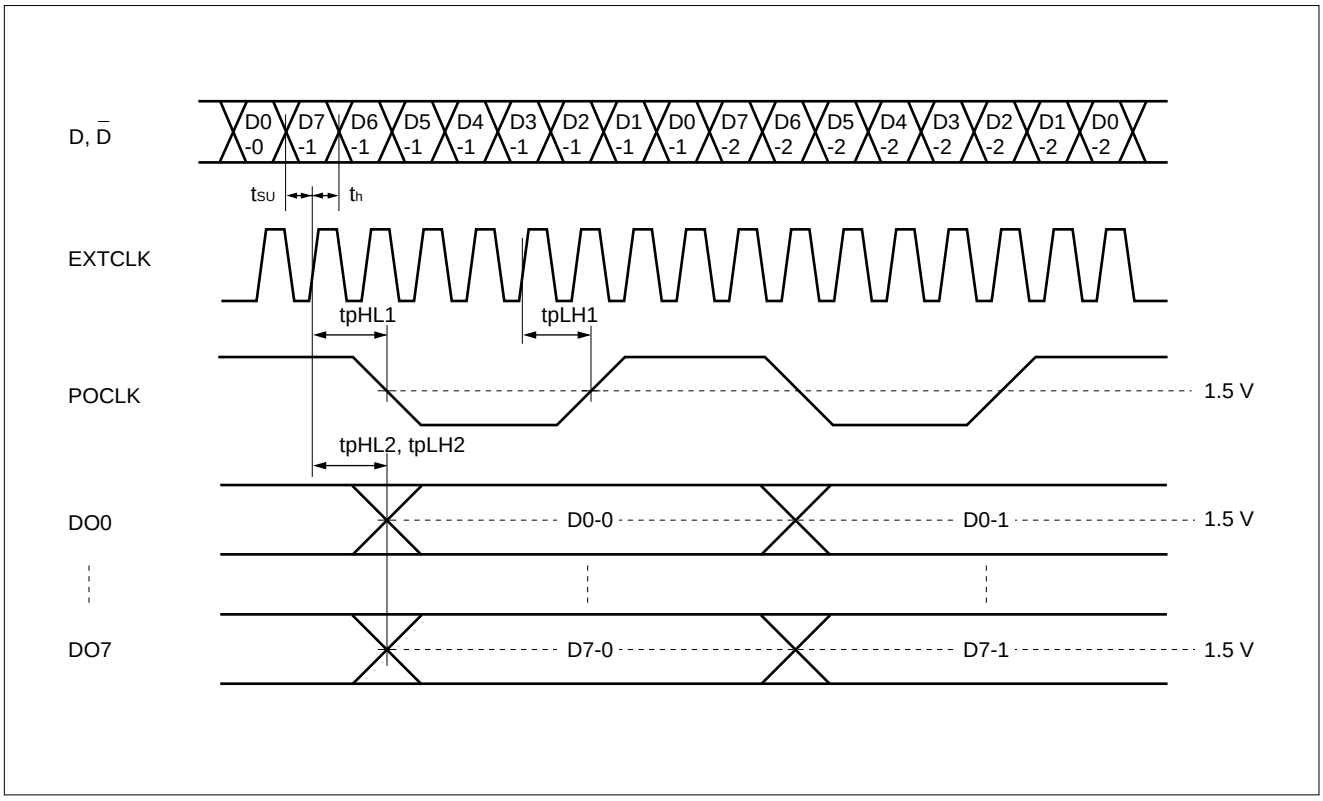


- **External serial clock input timing**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
EXTCLK ↔ D, $\overline{D}$	Setup time	t_{SU}	CLKSEL = “0”	1.5	—	—	ns
	Hold time	t_h		1.5	—	—	ns
EXTCLK → POCLK	Delay	tpHL1	CLKSEL = “0”	—	15.0	—	ns
	Delay	tpLH2		—	15.0	—	ns
EXTCLK → DO0 to DO7	Delay	tpHL2	CLKSEL = “0”	—	15.0	—	ns
	Delay	tpLH2		—	15.0	—	ns

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

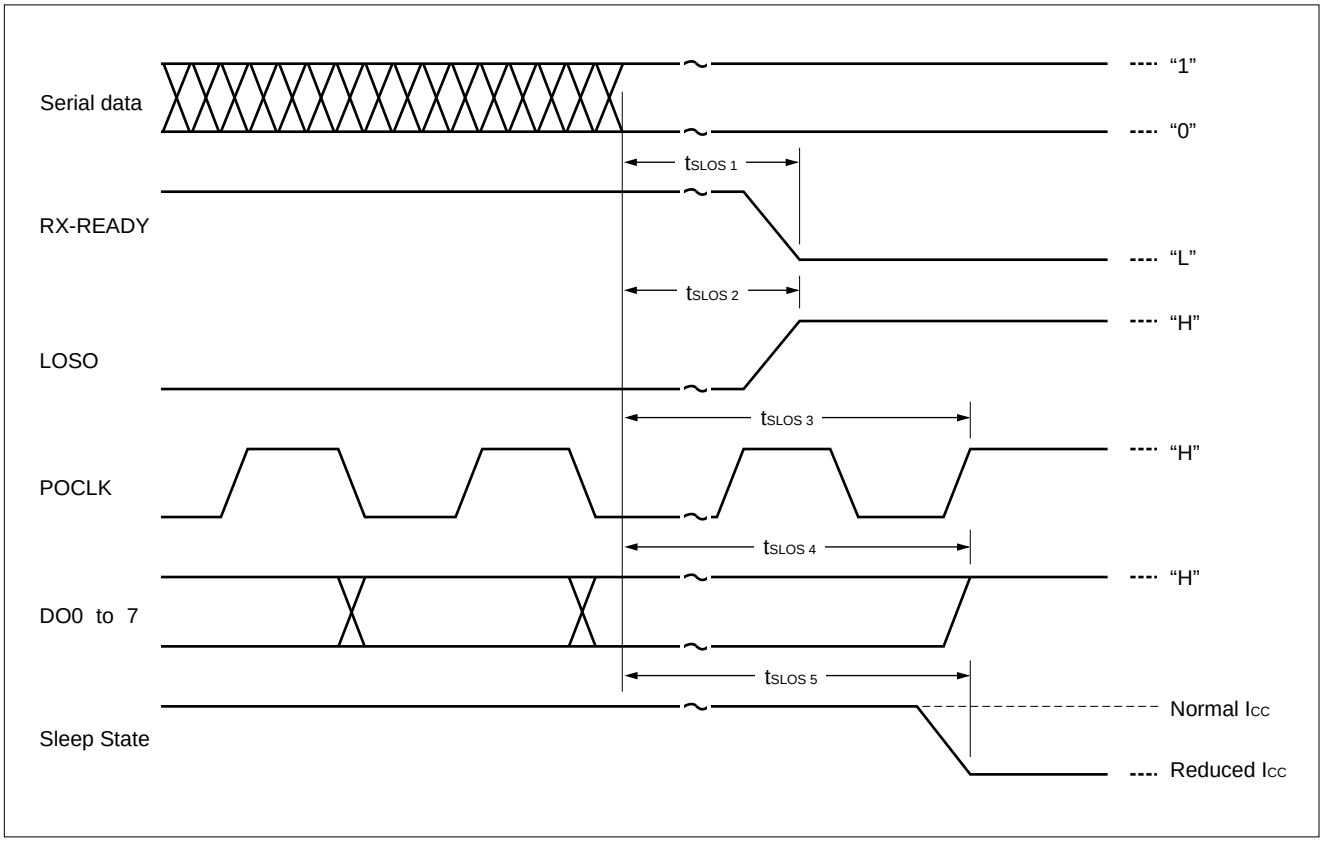


- **Loss-state serial data timing**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
Serial data loss state → RX-READY	Delay	t_{SLOS1}	—	—	2.5	—	µs
Serial data loss state → LOSO	Delay	t_{SLOS2}	—	—	2.5	—	µs
Serial data loss state → POCLK	Delay	t_{SLOS3}	—	—	10	—	µs
Serial data loss state → DO0 to DO7	Delay	t_{SLOS4}	—	—	10	—	µs
Serial data loss state → Sleep state	Delay	t_{SLOS5}	—	—	10	—	µs

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

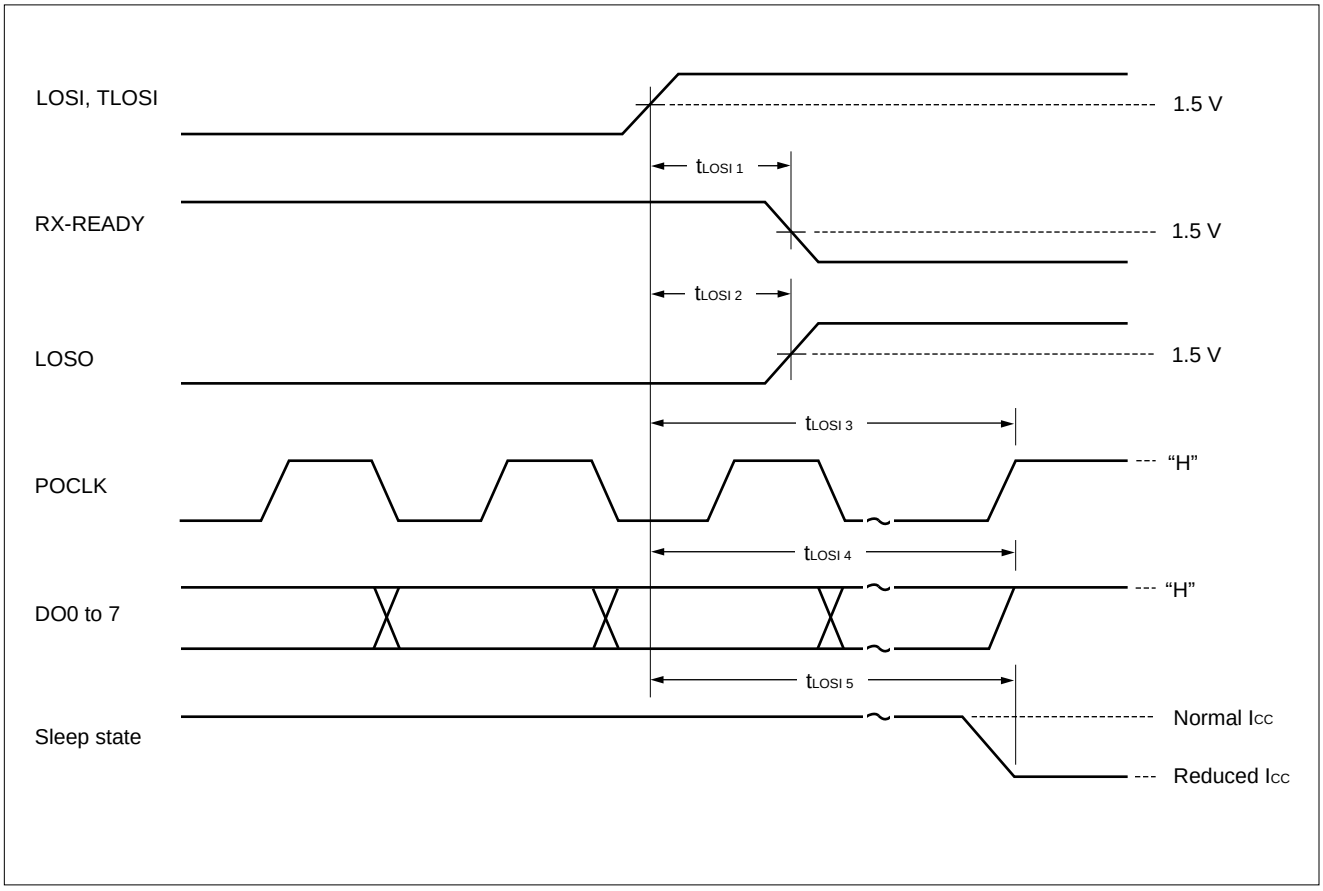


- **Loss signal timing**

(V_{CC} = +5.0 V ±5.0 %, Ta = –40°C to +85°C)

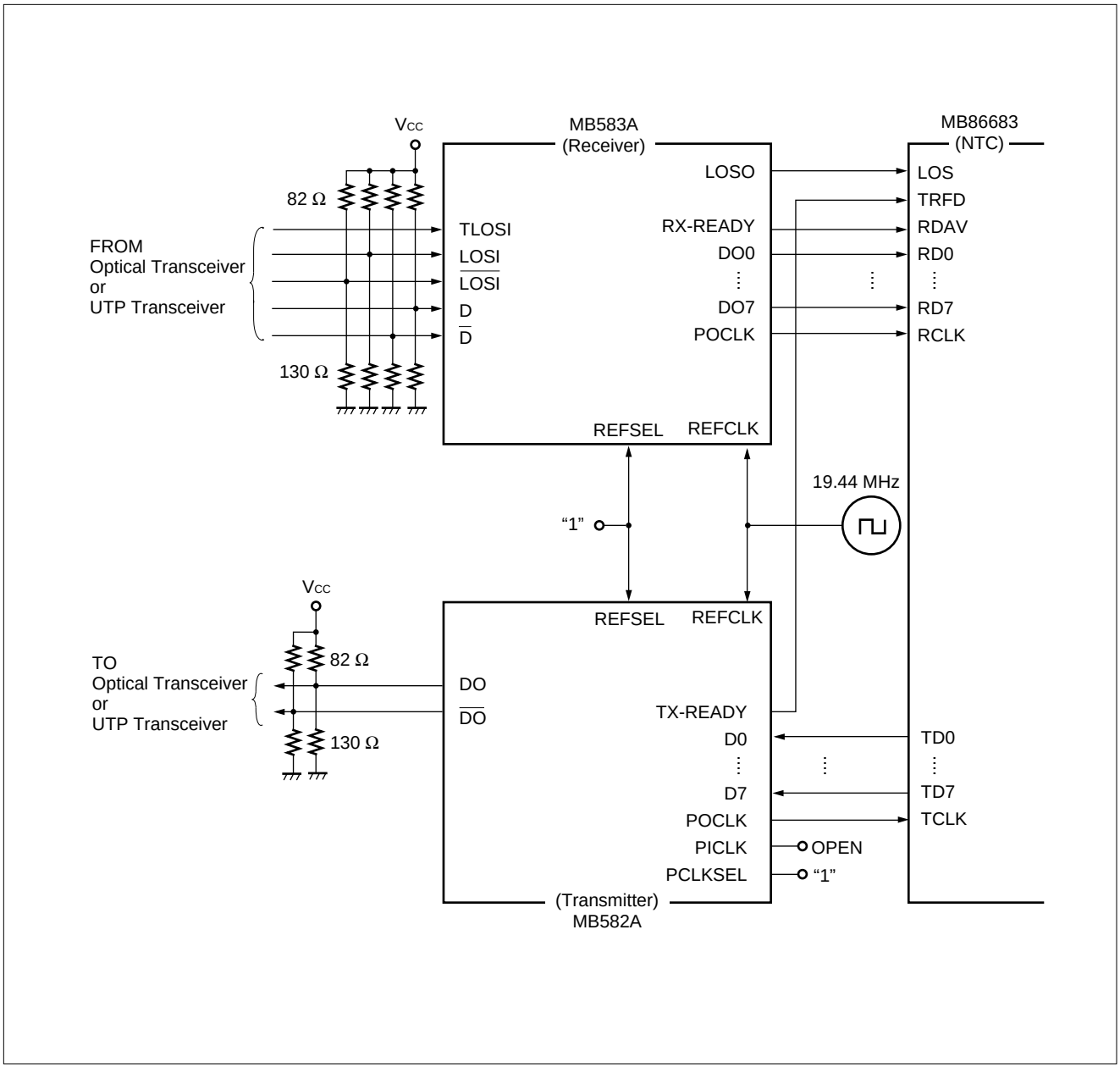
Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.*	Max.	
LOSI, TLOSI → RX-READY	Delay	t_{LOSI1}	—	—	20	—	ns
LOSI, TLOSI → LOSO	Delay	t_{LOSI2}	—	—	20	—	ns
LOSI, TLOSI → POCLK	Delay	t_{LOSI3}	—	—	7	—	µs
LOSI, TLOSI → DO0 to DO7	Delay	t_{LOSI4}	—	—	7	—	µs
LOSI, TLOSI → sleep mode	Delay	t_{LOSI5}	—	—	7	—	µs

* : Typical values assume that V_{CC} = +5.0 V and Ta = +25°C.

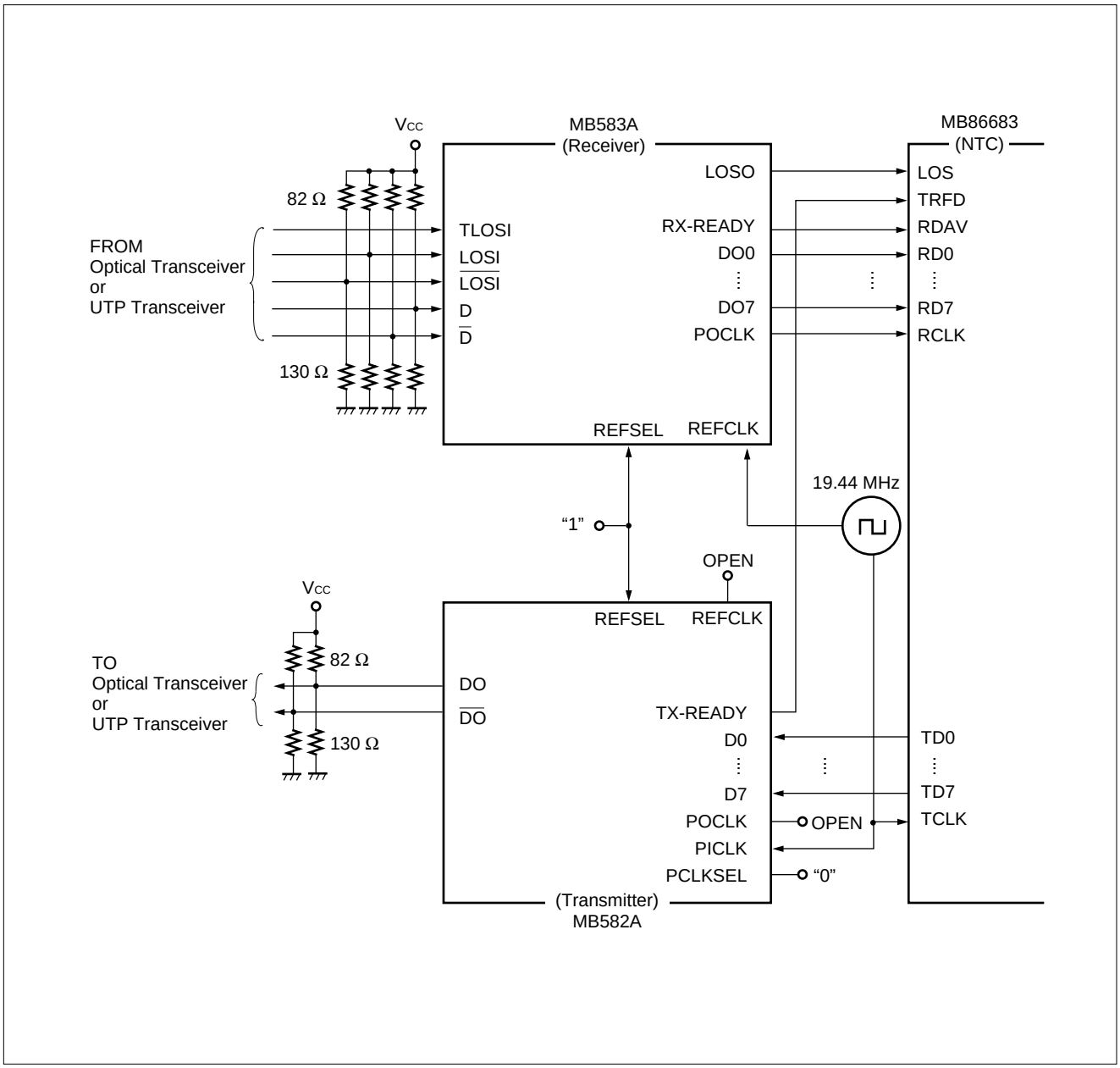


■ APPLICATION EXAMPLES

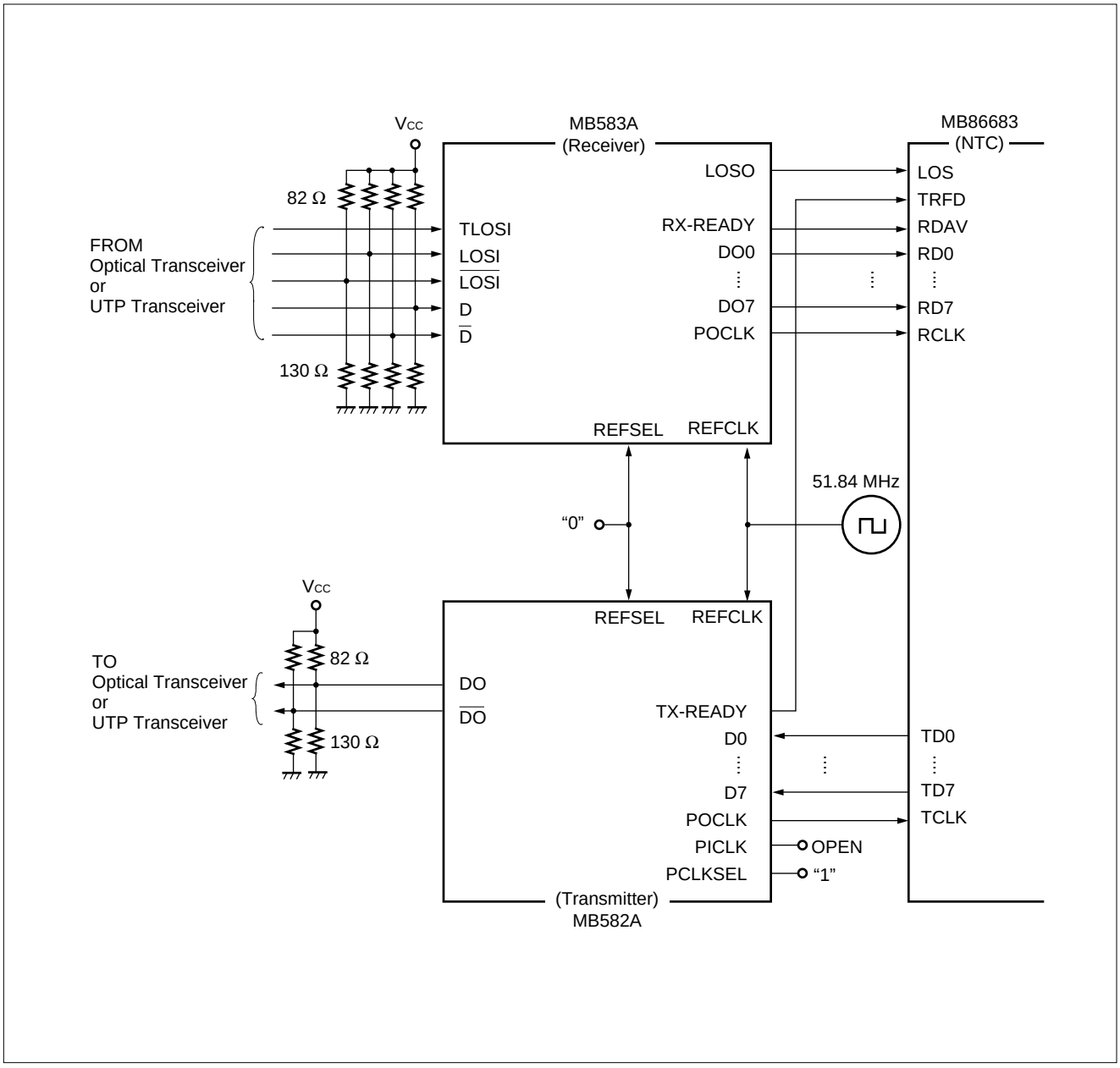
(1) When REFCLK = 19.44 MHz is used (without PICLK)



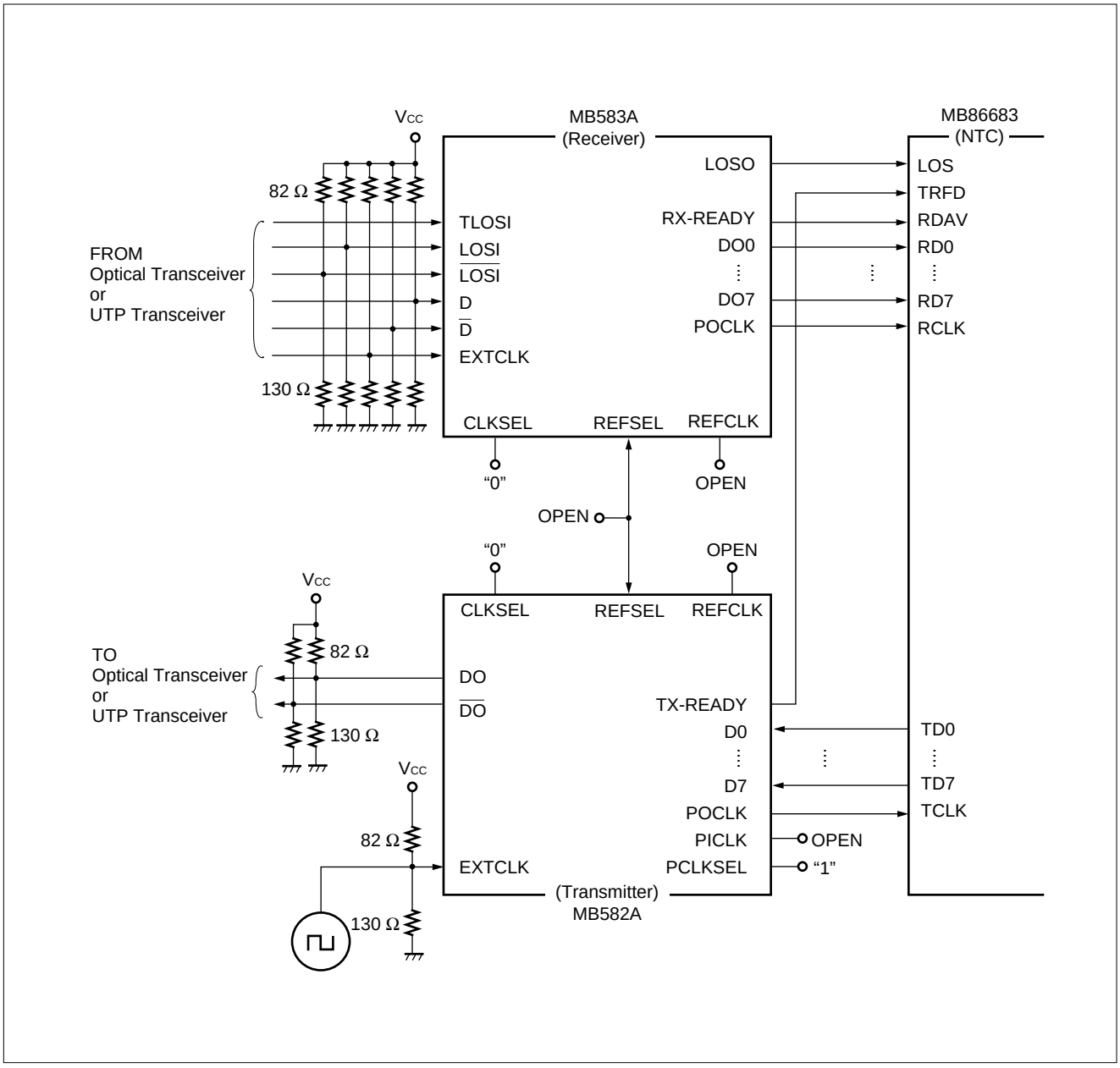
(2) When the MB582A uses PICLK = 19.44 MHz (without REFCLK) and the MB583A uses REFCLK = 19.44 MHz



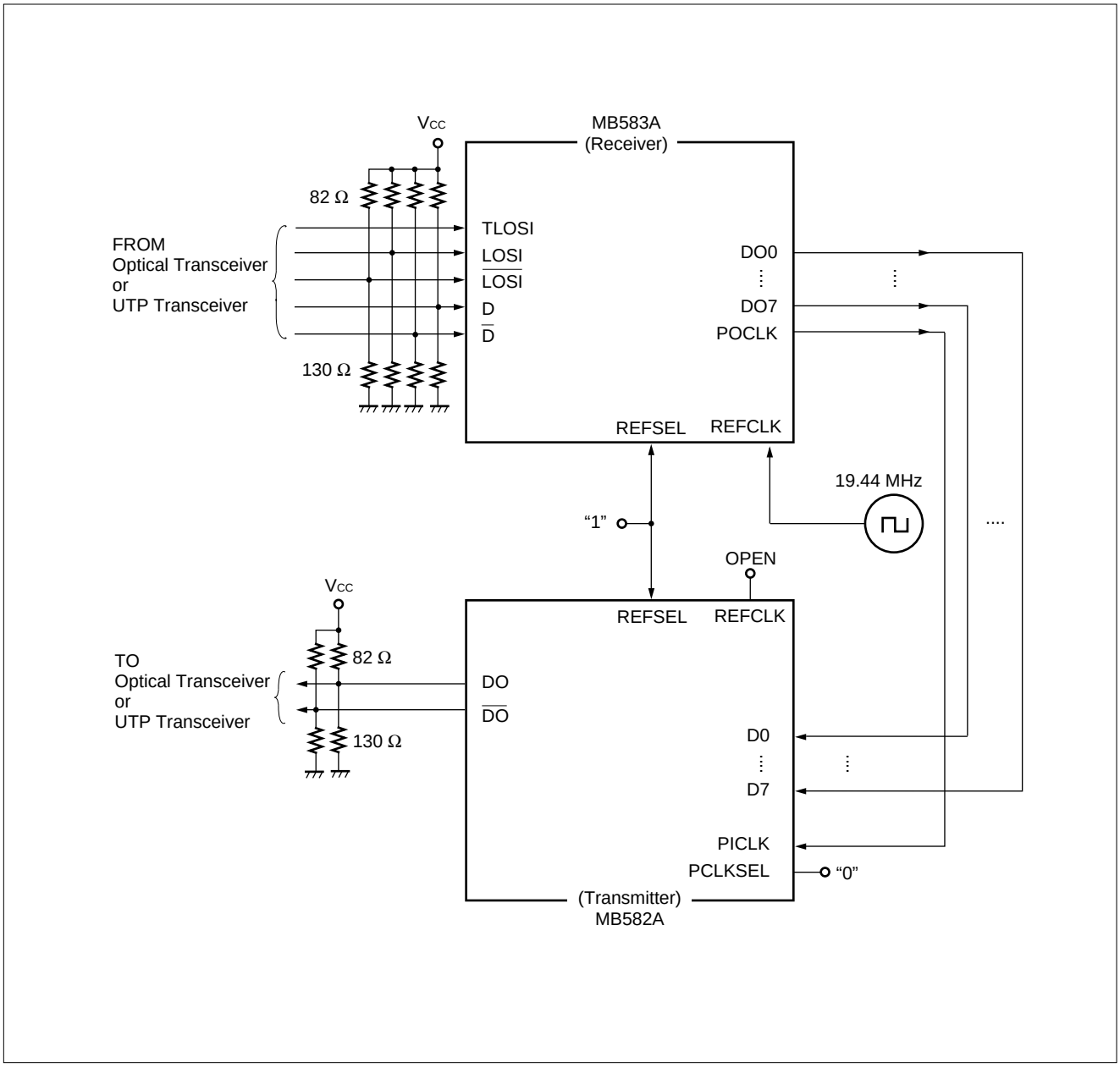
(3) When REFCLK = 51.84 MHz is used



(4) When the external clock is used

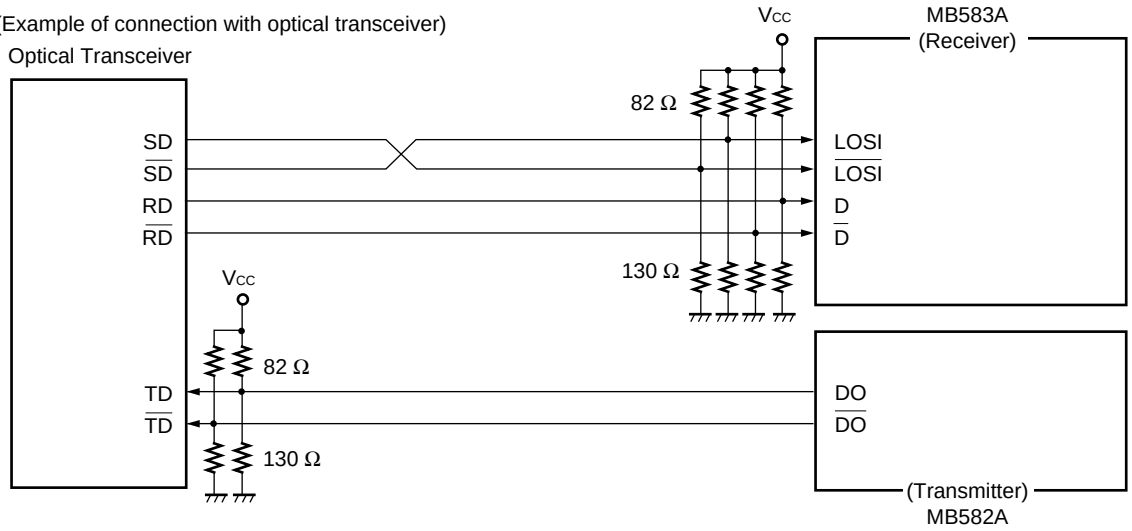


(5) When loopback is used

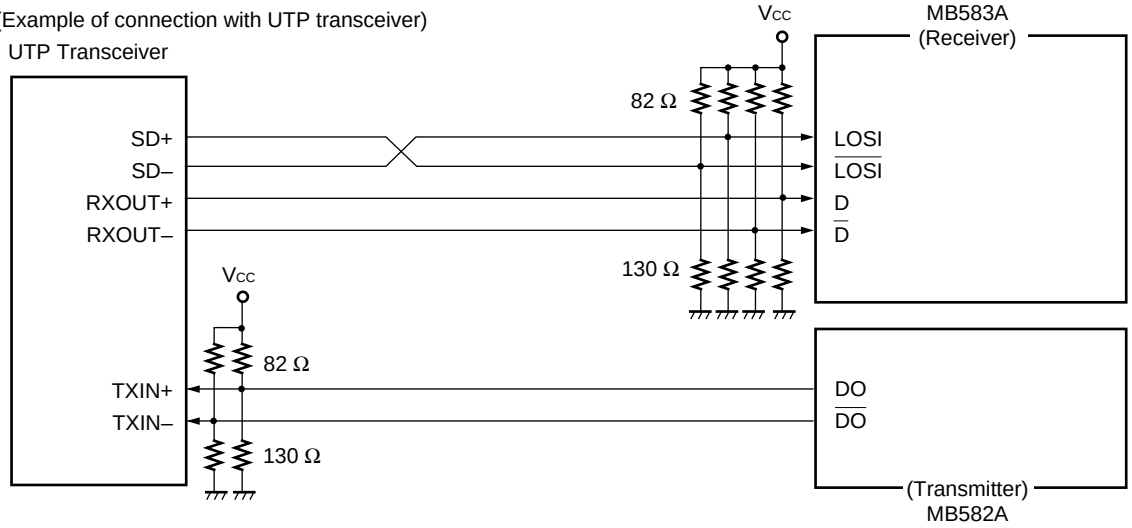


(6)

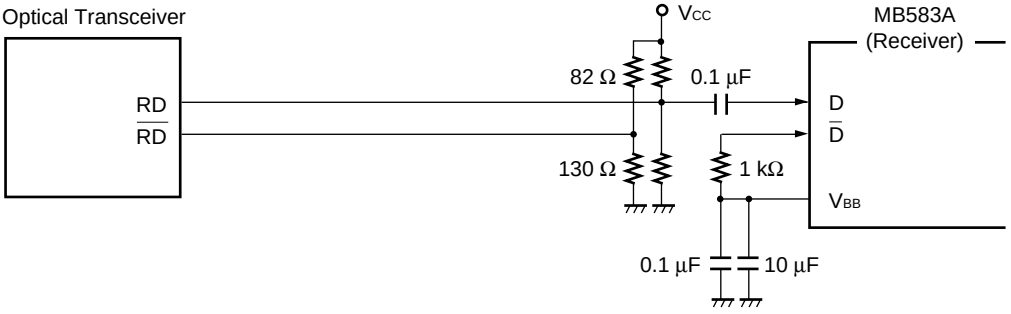
(Example of connection with optical transceiver)



(Example of connection with UTP transceiver)

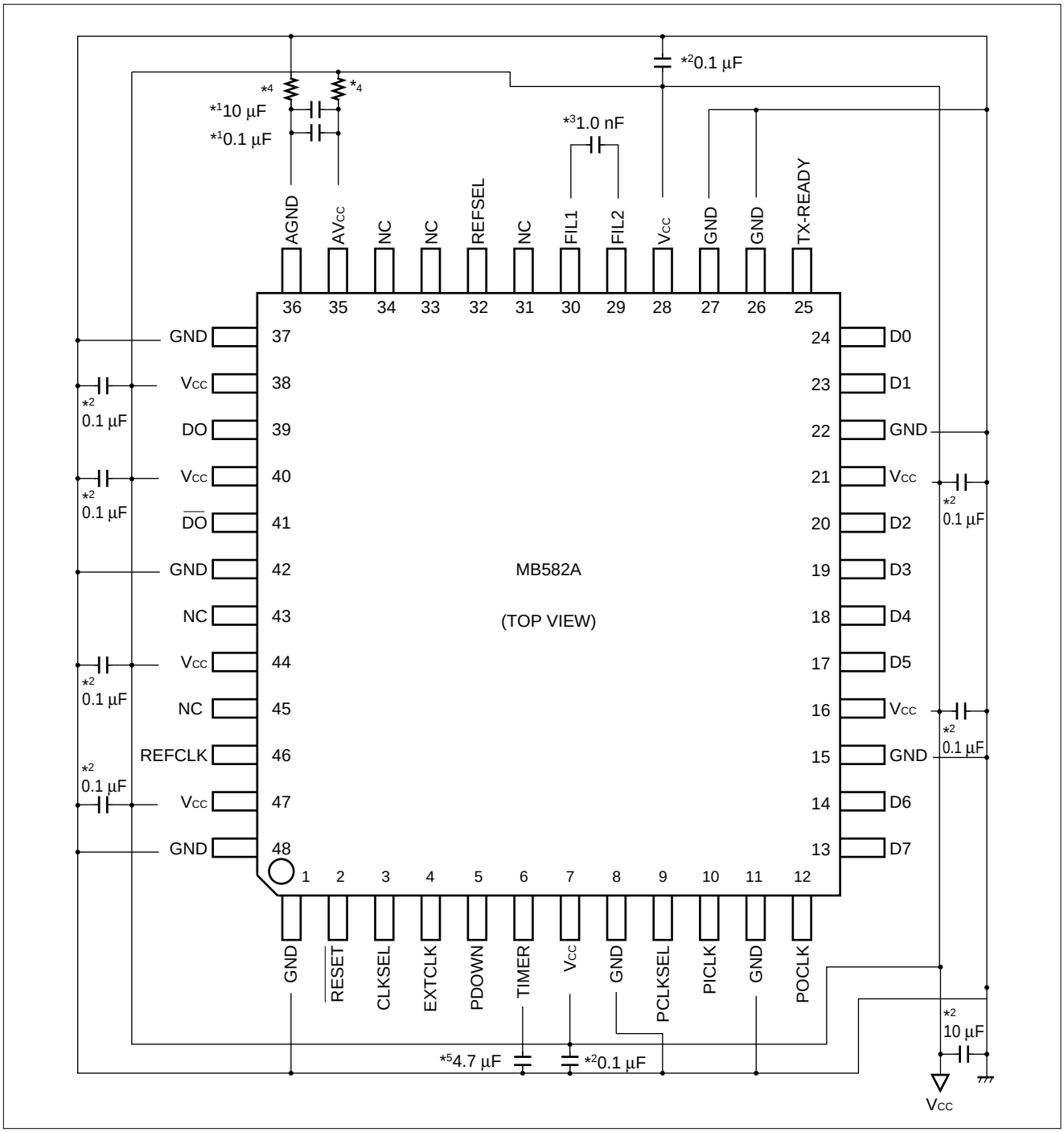


(Example of connection for a single input from optical transceiver to MB583A)



■ PERIPHERAL CIRCUITS

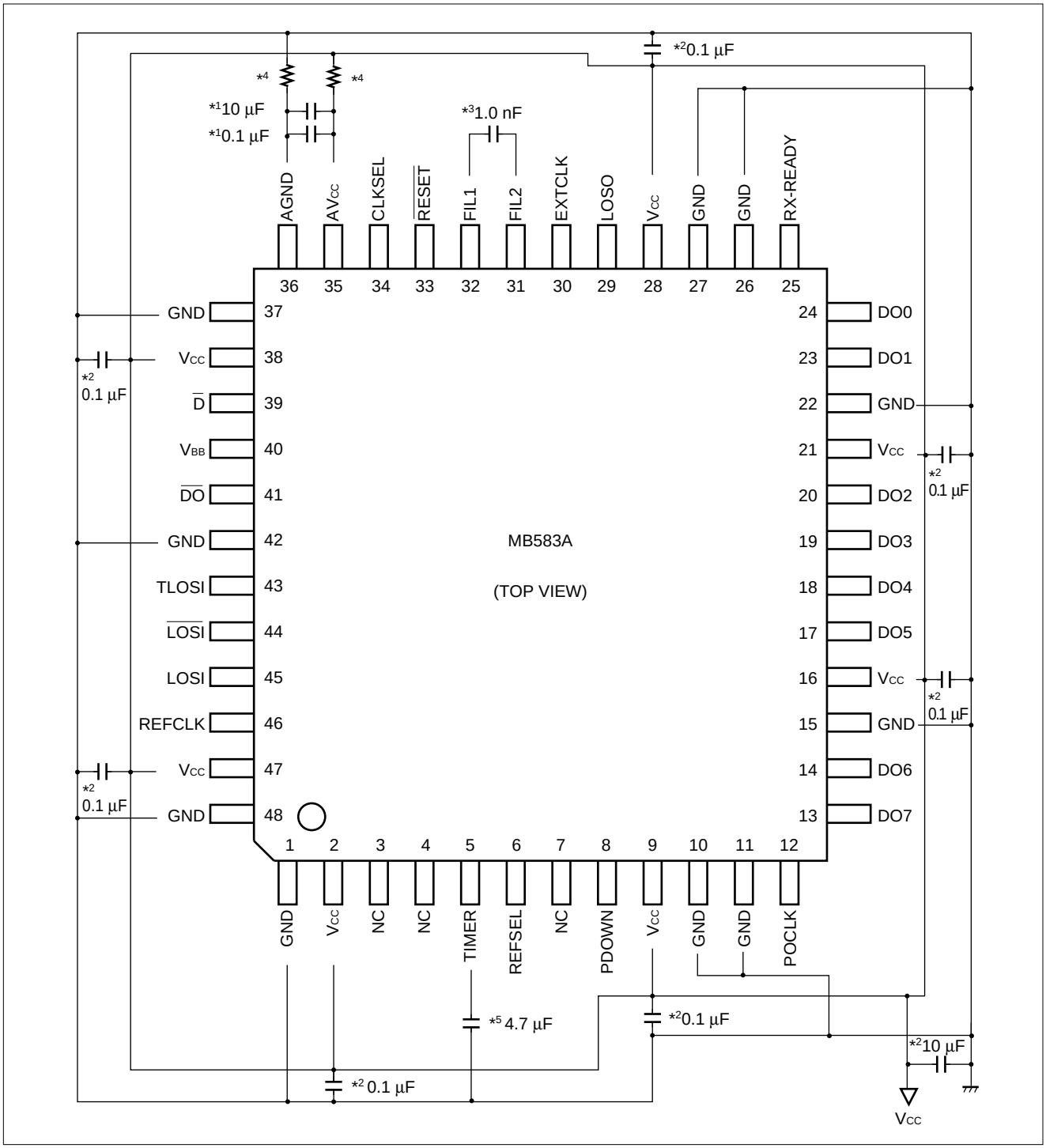
- **MB582A (Transmitter)**



*1: Bypass capacitor for power supply, connected between analog GND and analog V_{CC}.
*2: Bypass capacitor for power supply, connected between digital GND and digital V_{CC}.
*3: Filter capacitor.
*4: Although resistance is 0 Ω, reserve AGND and AV_{CC} patterns.
*5: Capacitor for power-on reset.

Note: External elements should be located as closer to the relevant pins as possible.

- **MB583A (Receiver)**



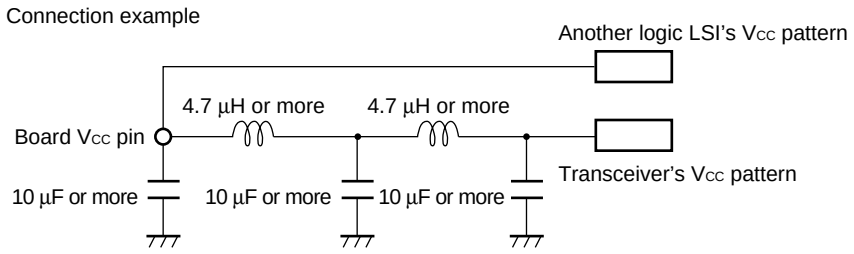
*1: Bypass capacitor for power supply, connected between analog GND and analog V_{CC}.
*2: Bypass capacitor for power supply, connected between digital GND and digital V_{CC}.
*3: Filter capacitor.
*4: Although resistance is 0 Ω, reserve AGND and AV_{CC} patterns.
*5: Capacitor for power-on reset.

Note: External elements should be located as closer to the relevant pins as possible.

■ PRECAUTIONS

(1) For the V_{CC} supplied to the MB582A/583A, use a stable power supply. If spike noise enters the power supply, the MB582A/583A may fail to perform stable operation.

1-1. The power supply for this LSI should be separated from the power supply for any other LSI not to receive digital noise (as shown in the following illustration).



Note: Suppress the total voltage drop by the inductor to be 50 mV or less.
(Inductor allowable current = 0.5 A or more; Inductor total DC resistance = 0.1 Ω or less)

1-2. To prevent spike noise from another LSIs, add sufficient capacitance also to another LSIs (for example, 10 µF for each of the LSIs).

1-3. Connect a bypass capacitor of about 0.1 µF closer (as within 10 mm as possible) to the pins between each V_{CC} and GND.

Between AV_{CC} and AGND which are an analog V_{CC} and an analog GND, in particular, connect a bypass capacitor closer (within 10 mm) to the LSI pins.

For the power source, attach a capacitor with a large value of about 10 µF to provide stable power.

(2) A external filter capacitor between FIL1 and FIL2 must be placed closer (as within 15 mm as possible) to the LSI pins. This capacitor must be wired by minimum routing. The wiring should not cross any other pattern. The pins are particularly sensitive to external noise. Placing this capacitor at lower-noise positions ensure their stable operations. In addition, routing GND patterns around the pins and the capacitor greatly contributes to stable operation.

(3) Letting the wiring for reference clock signals supplied to the REFCLK and PICLK cross other patterns increases jitter, leading to unstable operation.
Note also that input of a reference clock signal with large undershoot results in unstable operation.

(4) Serial data signals are transmitted at a high speed of 155.52 Mbps. Pay attention to the following points:

4-1. Connect a serial data terminal resistor of 82 Ω to the V_{CC} and of 130 Ω to the GND. Connect these terminal resistors closer to the receiving device side. (Placing a terminal resistor far away from the receiving device causes signal reflection, resulting in degradation of serial data.)

4-2. The serial data transmission line must have 50 Ω impedance. (Inappropriate line impedance causes signal reflection, resulting in degradation of serial data.)

4-3. Do not bend the serial data transmission line with 90°. Also, do not pass it through a through hole. (The through hole causes an impedance mismatch.)

4-4. The serial data transmission line should be minimum routed.

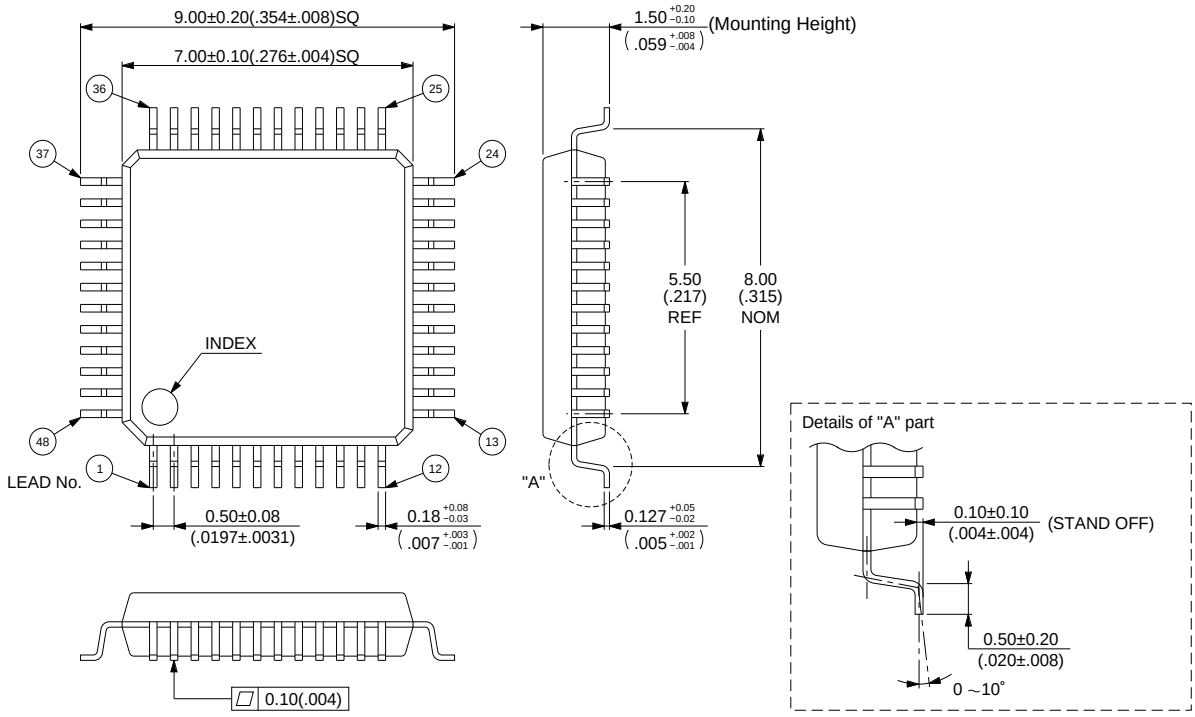
(5) Taking account of the above points, the board plane should be a four or more layers.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB582APFV	48 pin Plastic SQFP (FPT-48P-M05)	
MB583APFV		

■ PACKAGE DIMENSION

48 pin, Plastic LQFP
(FPT-48P-M05)



Dimensions in mm(inches).

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